Vivado Design Suite Hands-on Introductory Workshop

FPGA 2

VIVA12000-ILT (v1.0)

Course Specification

Course Description

This course offers introductory training on the Vivado® Design Suite. This course is for experienced ISE® Design Suite users who want to take full advantage of the Vivado Design Suite feature set. Learn about the Vivado Design Suite projects, design flow, Xilinx Design Constraints (XDC), and basic timing reports.

Level – FPGA 2

Course Duration – 1 day

Price – $800 or 8 Xilinx Training Credits

Course Part Number – VIVA12000-ILT

Who Should Attend? – Existing Xilinx ISE software Project Navigator FPGA designers

Prerequisites

- FPGA design experience
- Completion of *Essentials of FPGA Design* or equivalent knowledge of the Xilinx ISE Design Suite implementation tools
- Intermediate VHDL or Verilog knowledge

Recommended

- *Essential Tcl Scripting for the Vivado Design Suite* course

Software Tools

- Vivado Design or System Edition 2014.1

Hardware

- Architecture: 7 series FPGAs*
- Demo board: Kintex®-7 FPGA KC705 board*

* This course focuses on the 7 series architecture.

** Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Use the New Project wizard to create a new Vivado® IDE project
- Describe the supported design flows of the Vivado IDE
- Generate a DRC report to detect and fix design issues early in the flow
- Use the Vivado IDE I/O Planning layout to perform pin assignments
- Explore synthesis and implementation options and directives
- Synthesize and implement the HDL design
- Use the "baselining" process to gain timing closure on the design
- Generate the various reports at synthesis and implementation by using the Tcl Console and Flow Navigator to analyze the design
- Use the Schematic and Hierarchy viewers to analyze and cross probe the design
- Use the Vivado IDE IP flow to customize IP and generate the output products
- Differentiate between the XCI and DCP files in the Vivado IDE IP flow

Course Outline

- Vivado Synthesis and Implementation
- Performance Baselining
- Vivado Design Flows
- Demo: Vivado IDE Overview
- **Lab 1:** Vivado IDE Overview
- Demo: Vivado DRC, Synthesis, and Implementation
- **Lab 2:** Vivado Synthesis and Implementation
- **Lab 3:** Vivado Design Rule Checker
- Demo: Vivado Reports
- **Lab 4:** Vivado Reports
- Demo: Basic Design Analysis
- **Lab 5:** Basic Design Analysis
- Demo: Designing with the IP Integrator
- **Lab 6:** Designing with IP

Lab Descriptions

- **Lab 1:** Vivado IDE Overview – Create a project by using the New Project wizard in the Vivado IDE. Add files to the project by using the Add Sources wizard. Explore the Project Manager and Flow Navigator and simulate the design. Review the options available in the Flow Navigator.
- **Lab 2:** Vivado Synthesis and Implementation – Make timing constraints according to the design scenario. Modify synthesis and implementation settings. Synthesize and implement the design. Generate and download the bitstream to the demo board.
- **Lab 3:** Vivado Design Rule Checker – Run a DRC report on the elaborated design to detect design issues early in the flow. Fix the DRC violations.
- **Lab 4:** Vivado Reports – Generate the Timing Summary report and Clock Networks report on the synthesized design. Review the contents of the Timing Summary, Utilization, and Check Timing reports after implementing the design.
- **Lab 5:** Basic Design Analysis – Synthesize the design and use the Schematic and Hierarchy viewers to analyze the design. Implement the design and analyze some timing-critical paths with the Schematic viewer.
- **Lab 6:** Designing with IP – Generate an IP from the Vivado IP catalog. Customize and generate the output products for the IP. Review the DCP and XCI files. Instantiate the IP in the design.

Register Today

Morgan Advanced Programmable Systems, Inc. (MAPS, Inc.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota and Wisconsin.

Visit **morgan-aps.com/training**, for full course schedule and training information.

Morgan Advanced Programmable Systems

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.

- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

MAPS Inc. Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- MAPS may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is MAPS responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.