

VER2-ARCH (v1.0)

**Course Specification**

**Course Description**

Learn about the AMD Versal™ AI Edge Series Gen 2 and Prime Series Gen 2 adaptive SoC architectures, which combine programmable logic with a new high-performance processing system and next-generation AI Engines. Also learn how these devices facilitate end-to-end acceleration and maximize system performance for embedded systems—all in a single device built on a foundation of enhanced safety and security.

The emphasis of this course is on:

- Describing the different compute resources available in the Versal adaptive SoC
- Explaining the new high-performance processing system (PS)
- Describing the next-generation AI Engine architecture
- Describing the network on chip (NoC) resources
- Outlining the available DDR5/LPDDR5X memory controller support
- Reviewing the new image and video processing hard blocks
- Explaining the functional safety and security enhancements
- Identifying the available PCI Express® Gen 5 and 32G high-speed serial transceiver solutions

**What's New for 2025.2**

- Added new labs on:
  - Linux Application Development Using the Embedded Development Framework (EDF)
  - Generating the Hardware and Software Design Files for a Multimedia System
- All labs have been updated to the latest software versions

**Level – VER 1**

**Course Details**

- 2 days instructor led training (online or in person)
- 15 lectures
- 7 labs

**Price** – \$1,600 or 16 AMD Training Credits

**Course Part Number** – VER2-ARCH

**Who Should Attend?** – Software and hardware developers, system architects, and anyone who wants to learn about the architecture of the Versal AI Edge Series Gen 2 and Prime Series Gen 2 devices

**Prerequisites**

- Basic knowledge of AMD FPGAs and adaptive SoCs
- Basic knowledge of the AMD Vivado™ and Vitis™ tools

**Software Tools**

- [Vivado Design Suite 2025.2](#)
- [Vitis Unified IDE 2025.2](#)

**Hardware**

- Architecture: Versal adaptive SoC

After completing this comprehensive training, you will have the necessary skills to:

- Describe the different compute resources available in the AMD Versal adaptive SoC
- Explain the new high-performance processing system (PS)
- Describe the next-generation AI Engine architecture
- Describe the programmable network on chip (NoC) resources
- Outline the available DDR5/LPDDR5X memory controller support

- Describe the new image and video processing hard blocks
- Explain the functional safety and security enhancements
- Identify the available PCI Express Gen 5 and 32G high-speed serial transceiver solutions

**Course Outline**

**Day 1**

- **Introduction and Portfolio Overview**  
Describes the need for Versal devices and offers an overview of the Versal portfolio. {Lecture}
- **Architecture Overview**  
Provides a high-level overview of the Versal architecture, illustrating the various compute resources available in the Versal architecture. {Lecture}
- **Design Tool Flow**  
Maps the various compute resources in the Versal architecture to the tools required and describes how to target them for final image assembly. {Lecture, Lab}
- **Programmable Logic (PL)**  
Describes the logic resources available in the programmable logic. Also discusses the clocking architecture, clock buffers, clock routing, and clock de-skewing options. {Lecture}
- **SelectIO™ Resources**  
Describes the I/O bank, SelectIO interface, and I/O delay features. {Lecture}
- **Processing System**  
Reviews the Arm® Cortex®-A78AE processor APU and Cortex-R52 processor RPU that form the processing system. Discusses high-speed connectivity, boot modes, system peripherals, and power domains. Also introduces the AMD Embedded Development Framework (EDF) for streamlined application development. {Lecture, Lab}
- **Platform Management Controller (PMC)**  
Describes the platform management controller architecture and the role of platform loader and manager (PLM) in the Versal device boot process. {Lecture}
- **Boot and Configuration**  
Covers the boot phases, flows, and modes along with the process of generating a boot image. Also discusses the concept and benefits of segmented configuration. {Lecture}

**Day 2**

- **AIE-ML v2 Architecture Overview**  
Discusses the AI Engine AIE-ML v2 array architecture and its tiles. Also lists the key differences between the AIE, AIE-ML, and AIE-ML v2 architectures. {Lecture, Lab}
- **NoC Architecture**  
Covers the reasons to use the network on chip, the NoC architecture and its basic elements, design entry flows, and common terminology. {Lecture}
- **Designing with DDR5**  
Describes the DDR5 memory controller features and its configuration flow. Also demonstrates how to tune a design to increase efficiency. {Lecture, Lab}
- **Multimedia Hard Blocks**  
Reviews the multimedia-specific hard IP blocks such as VCU2, GPU, and ISP available in the Versal devices. {Lecture, Lab}

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- **Security and Functional Safety Overview**  
Describes the security architecture and the available security units. Also provides an overview of the increased embedded system security. {Lecture}
- **PCI Express Solutions**  
Provides an overview of the PCIe® module and describes the PL and MDB PCIe blocks. {Lecture, Lab}
- **Serial Transceivers**  
Describes the transceivers in the Versal device. Also introduces the new GT Wizard Subsystem flow. {Lecture, Lab}

- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person...for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly as planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your AMD based device quickly and efficiently.

**Register Today**

Morgan Advanced Programmable Systems, Inc. (Morgan A.P.S.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota, and Wisconsin.

Visit [morgan-aps.com/training](http://morgan-aps.com/training), for full course schedule and training information.



- You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and AMD training credits.

**Student Cancellation Policy**

- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent [here](#).

**Morgan A.P.S. Course Cancellation Policy**

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us [here](#).

**Online or in person training with real hardware**

- Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.