Designing with the Versal Adaptive SoC: Quick Start

VER-QSTART (v1.0)

Course Specification

Course Description

Explore the AMD Versal™ adaptive SoC heterogeneous architecture containing a programmable network on chip (NoC) and AI Engines and learn how to use different design tool flows targeting Versal devices. Gain knowledge of embedded software development and application partitioning. Also learn how to perform system migration to the Versal architecture.

The emphasis of this course is on:

- Reviewing the architecture of the Versal adaptive SoC
- Describing the different compute resources available in the Versal architecture
- Demonstrating the embedded software development flow for Versal devices
- Describing the architectures of the network on chip (NoC) and AI Engine
- Explaining application partitioning based on the models of computation
- Comparing various functional blocks of the Versal devices to previous-generation devices

What's New for 2025.2

- Embedded Software Development module: Added details on application development using the AMD Embedded Development Framework (EDF)
- All labs have been updated to the latest software versions

Level – VER 1

Course Details

- 1 day instructor led training (online or in person)
- 8 lectures
- 4 labs

Price – $800 or 8 AMD Training Credits

Course Part Number – VER-QSTART

Who Should Attend? – Software and hardware developers, system architects, and anyone who wants to learn about the architecture and programming of the Versal adaptive SoC

Prerequisites

- Basic knowledge of AMD FPGAs and adaptive SoCs
- Basic knowledge of the Vivado™ and Vitis tools

Recommended Training

- Designing with the Versal Adaptive SoC: Design Methodology

Software Tools

- Vivado Design Suite 2025.2
- Vitis Unified IDE 2025.2

Hardware

- Architecture: Versal adaptive SoC
- Demo board: Versal VCK190 Evaluation Platform

After completing this comprehensive training, you will have the necessary skills to:

- Describe the AMD Versal architecture
- Describe the Versal design flows
- Describe the embedded software development flow for Versal devices
- Design using the network on chip (NoC)
- Create a simple AI Engine application
- Follow the high-level system migration recommendations provided in this course

Course Outline

- **Introduction and Portfolio Overview**
  Describes the need for Versal devices and offers an overview of the Versal portfolio. {Lecture}
- **Architecture Overview**
  Provides a high-level overview of the Versal architecture, illustrating the various compute resources available in the Versal architecture. {Lecture}
- **Design Tool Flow**
  Maps the various compute resources in the Versal architecture to the tools required and describes how to target them for final image assembly. {Lecture, Lab}
- **Embedded Software Development**
  Describes the software development environments and embedded software development flows for Versal devices. Also introduces embedded software debugging. {Lecture, Lab}
- **NoC Introduction and Concepts**
  Covers the reasons to use the network on chip, its basic elements, design entry flows, and common terminology. {Lecture, Lab}
- **AI Engine**
  Discusses the AI Engine array architecture, terminology, and AI Engine interfaces. {Lecture, Lab}
- **Application Mapping and Partitioning**
  Covers the system design methodology and describes how different models of computation (sequential, concurrent, and functional) can be mapped to the Versal adaptive SoC. Also describes what application partitioning is and how an application can be accelerated by using the various compute domains in the Versal device. {Lecture}
- **System Migration**
  Compares the various functional blocks of the Versal devices to previous-generation devices. Describes the migration of designs from the UltraScale™ and UltraScale+™ architectures to the Versal architecture. {Lecture}

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Online or in person training with real hardware

- Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your AMD based device quickly and efficiently.