Designing with the Versal Adaptive SoC: PCI Express Systems

VER-PCIE (v1.0)

Course Specification

Course Description

This course introduces the features and capabilities of the PCIe® and Cache Coherent Interconnect blocks in the AMD Versal™ adaptive SoC architecture. Learn how to implement a Versal device PCI Express® solution in custom applications to improve time to market.

The emphasis of this course is on:

- Describing the PCI Express design methodology for Versal devices
- Reviewing various Versal device PCI Express core products
- Selecting the PCI Express IP cores from the Vivado™ Design Suite
- Generating PCI Express example designs and simple applications
- Identifying the advanced capabilities of the PCIe specification

This course also focuses on the AXI-Streaming interconnect.

What's New for 2025.1

- Updated to Versal Prime Series Gen 2 and Versal AI Edge Series Gen 2
- New content on Gen 2 Series PS MDB PCI Express Solution
- All labs have been updated to the latest software versions

Level – Connectivity 3

Course Details

- 2 days instructor led training (online or in person)
- 20 lectures
- 8 labs

Price – $1600 or 16 AMD Training credits

Course Part Number – VER-PCIE

Who Should Attend?

- Hardware designers who want to create applications using Versal device IP cores for PCI Express
- Software engineers who want a deeper understanding of the Versal device PCI Express solutions
- System architects who want to leverage key Versal device advantages related to performance, latency, and bandwidth in PCI Express applications

Prerequisites

- Experience with the PCI/PCIe specification protocol
- Knowledge of VHDL or Verilog
- Experience with the Vivado Design Suite
- Designing with the Versal Adaptive SoC: Design Methodology
- Moderate digital design experience

Software Tools

- Vivado Design Suite 2025.1

Hardware

- Architecture: Versal adaptive SoC

After completing this comprehensive training, you will have the necessary skills to:

- Construct a basic PCI Express system by:
  - Selecting the appropriate IP for your application
  - Specifying the requirements of an endpoint application
  - Connecting PCIe IPs with the user application
  - Utilizing programmable logic (PL) and processing system (PS) resources supporting PCI Express
  - Simulating and implementing PCI Express systems
- Identify the advanced capabilities of the PCI Express specification protocol and feature set

Course Outline

Day 1

- **Introduction to PCI Express**
  Introduces the course and discusses a few key topics of the PCI Express protocol. {Lecture, Lab}
- **Versal Adaptive SoC PCIe Solutions Overview**
  Provides an overview of the PCI Express solutions in the Versal architecture and identifies key differentiators. {Lecture}
- **PCIe Block Architecture and Functionality**
  Describes the PL PCIe block architecture. You will learn details on the block features and functionality. {Lecture}
- **PCIe Block Interfaces Overview**
  Provides an overview of the PL PCIe block interfaces. Deeper discussion on physical layer and general interfaces. {Lecture}
- **PCIe Block Requester Interfaces**
  Reviews the requester AXI4-Streaming core interfaces. You will learn how to utilize packet descriptors for request interfaces. {Lecture}
- **PCIe Block Completer Interfaces**
  Reviews the completer AXI4-Streaming core interfaces. You will learn how to utilize packet descriptors for completion interfaces. {Lecture, Lab}
- **PHY for PCI Express**
  Describes the Versal device PHY for PCI Express IP architecture and interfaces. You will learn how to utilize this soft IP in PCI Express designs. {Lecture}
- **PCIe Block Customization**
  Illustrates customizing the PL PCIe block. You will learn how to utilize the various configuration options. {Lecture, Lab}
- **PCIe Block Test Bench and Simulation**
  Discusses PCIe block simulation. You will learn how to utilize the generated example design to verify the functionality of the PL PCIe solution. {Lecture, Lab}

Day 2

- **PCIe Block Implementation**
  Discusses implementation topics. You will review the placement recommendations for the PL PCIe blocks, transceivers, clocks, and resets. {Lecture, Lab}
- **PL PCIe Block Debugging Overview**
  Describes the PCI Express debugging options in the Versal device PCI Express physical and transaction layers. You will learn how to perform PCI Express link debug. {Lecture, Lab}
- **CPM Architecture and Functionality**
  Describes the CPM block architecture and functionality. You will learn the commonalities and differences to the PL PCIe solution. {Lecture}
- **CPM Block Customization**
  Reviews the configuration options of the CIPS CPM block. You will learn how to customize the CPM PCIe block. {Lecture}
- **CPM IP Use Cases**

Describes typical use cases for the Versal device PCI Express solutions to enable you to select the right solution for your design requirements. {Lecture, Lab}

- **MDB Architecture and Functionality**
  Describes the MDB block architecture and functionality. You will learn the commonalities and differences to the Gen 1 devices PCIe solution. {Lecture}
- **MDB Block Customization**
  Reviews the configuration options of the MDB block. You will learn how to customize the BDM PCIe block. {Lecture}
- **Introduction to DMA**
  Reviews DMA basics and describes DMA in the context of the PCI Express standard. {Lecture}
- **PL PCIe XDMA/Bridge Subsystem**
  Describes the Versal device XDMA architecture and features as well as DMA descriptor usage and interface options. You will learn how to utilize the XDMA subsystem. {Lecture, Lab}
- **PL PCIe QDMA Subsystem**
  Describes the Versal device QDMA architecture and features. You will learn how to utilize the QDMA subsystem and its queue usage. {Lecture}
- **PS MDB DMA Solution**
  Describes the Gen2 series Hyper DMA architecture and features. {Lecture}

Register Today

Morgan Advanced Programmable Systems, Inc. (Morgan A.P.S.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota, and Wisconsin.

Visit **morgan-aps.com/training**, for full course schedule and training information.

Morgan Advanced Programmable Systems

- You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and AMD training credits.

Student Cancellation Policy

- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

Morgan A.P.S. Course Cancellation Policy

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.

Online or in person training with real hardware

- Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your AMD based device quickly and efficiently.