

## Course Description

This course introduces the AMD Versal™ network on chip (NoC) to users familiar with other SoC architectures. Besides providing an overview of the major components in the Versal device, the course illustrates how the NoC can be configured to access DDR memory controllers and HBM memory controllers.

The emphasis of this course is on:

- Enumerating the major components comprising the NoC architecture in the Versal adaptive SoC
- Implementing a basic Versal NoC design using the Vivado™ IP integrator
- Accessing the Versal NoC using the modular NoC flow
- Configuring the DDR memory controller for accessing DDR memory
- Configuring and tuning the NoC for efficient data movement

### What's New for 2025.2

- Added a new module on NoC DDR5 Memory Controller
- All labs have been updated to the latest software versions

Level – VER 2

#### Course Details

- 1 day instructor led training (online or in person)
- 9 lectures
- 5 labs

Price – \$800 or 8 AMD Training Credits

Course Part Number – VER-NOC

**Who Should Attend?** – Hardware developers and system architects—whether migrating from existing AMD SoC devices or starting out with the Versal devices

#### Prerequisites

- Any SoC or Versal adaptive SoC architecture course
- [Designing with the Versal Adaptive SoC: Design Methodology](#)
- Familiarity with the [Vivado™ Design Suite](#)
- Familiarity with the Vitis™ Unified IDE

#### Software Tools

- [Vivado Design Suite 2025.2](#)
- [Vitis Unified IDE 2025.2](#)

#### Hardware

- Architecture: Versal adaptive SoCs

After completing this comprehensive training, you will have the necessary skills to:

- Identify the major network on chip components in the AMD Versal architecture
- Include the necessary components to access the NoC from the PL
- Access the Versal NoC resources using the IP integrator and/or modular NoC flow
- Design with the NoC and integrated DDR memory controller
- Configure connection QoS for efficient data movement

## Course Outline

- **Architecture Overview for Existing Users**  
Introduces to students who already have familiarity with AMD SoC architectures the new and updated features found in the Versal

devices. Also provides an overview of the Versal portfolio. {Lecture}

- **NoC Introduction and Concepts**  
Covers the reasons to use the network on chip, its basic elements, design entry flows, and common terminology. {Lecture, Lab}
- **NoC Architecture**  
Provides a deep dive into the sub-blocks of the NoC and how they are used. Describes how the NoC is accessed from the programmable logic. {Lecture}
- **Design Tool Flow**  
Maps the various compute resources in the Versal architecture to the tools required and describes how to target them for final image assembly. {Lecture}
- **Modular NoC Flow**  
Introduces the modular NoC flow for accessing Versal NoC resources. Also discusses modular NoC flow-supported use cases. {Lecture, lab}
- **NoC DDR4 Memory Controller**  
The integration between the NoC pathways and the DDR4 memory controllers must be understood to have efficient data movement on and off chip. This discussion of the NoC's DDR4 memory controller blocks provides the background for properly selecting and configuring DDR4 memory and the memory controller for effective use. {Lecture, Lab}
- **NoC DDR5 Memory Controller**  
The integration between the NoC pathways and the DDR5 memory controllers must be understood to have efficient data movement on and off chip. This discussion of the NoC's DDR5 memory controller blocks provides the background for properly selecting and configuring DDR5 memory and the memory controller for effective use. {Lecture, Lab}
- **NoC HBM Controller**  
Describes the high-bandwidth memory (HBM) controller architecture and identifies the steps for HBM controller configuration. {Lecture}
- **NoC Performance Tuning**  
Synthesizes everything about the NoC and its DDRMCs, illustrating how to fine tune the NoC for the best performance. {Lecture, Lab}

## Register Today

Morgan Advanced Programmable Systems, Inc. (Morgan A.P.S.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota, and Wisconsin.

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- You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and AMD training credits.

## Student Cancellation Policy

- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent [here](#).

### **Morgan A.P.S. Course Cancellation Policy**

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us [here](#).

### **Online or in person training with real hardware**

- Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person...for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly as planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your AMD based device quickly and efficiently.