Designing with the Versal Adaptive SoC: Memory Interfaces

VER-MEM (v1.0)

Course Specification

Course Description

This course provides a system-level understanding of AMD Versal™ adaptive SoC memory interfaces. Memory controller architecture, IP generation, simulation, and implementation are covered. Additional information on PCB design issues is also covered.

The focus is on:

- Constructing a system using Versal adaptive SoC external memory interfaces by:
  - Selecting the appropriate IP for an application
  - Configuring the memory controller IPs
  - Using the memory controllers in test benches and applications
  - Simulating and implementing the memory controller IPs
- Exploring traffic pattern generation
- Performance tuning for the hardened DDRMC
- Accessing the appropriate reference material for board design issues involving signal integrity, the power supply, reference clocking, and trace design

What's New for 2025.1

- New DDR5/LPDDR5 module with DDRMC5 content added
- New labs for DDRMC5 interface generation and simulation
- All labs have been updated to the latest software versions

Level – VER 3

Course Details

- 2 days instructor led training (online or in person)
- 13 lectures
- 5 labs on DDR4 and 5 labs on DDR5

Price – $1,600 or 16 AMD Training Credits

Course Part Number – VER-MEM

Who Should Attend?

- Hardware designers who want to create applications using external memory devices or modules
- System architects who want to leverage the key advantages of external memory interfaces

Prerequisites

- Knowledge of Verilog or VHDL
- Familiarity with logic design (state machines and synchronous design)
- Some experience with Vivado™ implementation
- Some experience with a simulation tool (preferably the Vivado simulator)
- Familiarity with DDR or LPDDR memories also helpful

Software Tools

- Vivado Design Suite 2025.1
- Vitis Unified IDE 2025.1

Hardware

- Architecture: All Versal adaptive SoC devices
- Evaluation board: Versal adaptive SoC VCK190 Evaluation Platform

After completing this comprehensive training, you will have the necessary skills to:

- Describe and utilize the building blocks of the hardened DDR memory controllers in AMD Versal devices
- Describe and utilize the ports and attributes of the hardened memory controllers
- Design, simulate, and implement designs using the hardened memory controllers
- Utilize DDR4/LPDDR4 debugging options
- Apply performance tuning options for linear and random traffic
- Identify memory interface board design requirements

Course Outline

Day 1

- **Versal Adaptive SoC: Architecture Overview for Existing Users**
  Introduces to students who already have familiarity with AMD SoC architectures the new and updated features found in the Versal devices. Also provides an overview of the Versal portfolio. {Lecture}
- **Network on Chip**
  Provides a deep dive into the sub-blocks of the NoC and how they are used. Describes how the NoC is accessed from the programmable logic. {Lecture}
- **Memory Solutions Overview**
  Identifies the external memory interfaces options for the Versal adaptive SoC and describes the main features of the hard and soft controllers. {Lecture}
- **DDR4 and LPDDR4 Memories**
  Discusses the DDR4 architectural and interface improvements and describes the LPDDR4 differences from DDR4. {Lecture}
- **DDR5 and LPDDR5 Memories**
  Reviews the DDR5/LPDDR5 architectural and interface improvements. {Lecture}
- **Hardened DDR Memory Controllers**
  Describes the architecture and functionality of the hardened DDR memory controllers and the PHY block. {Lecture}
- **Configuring the Hardened DDR Memory Controllers**
  Covers how to perform hardened DDR memory controller configuration and provides background information for selecting optimal parameters. {Lecture, Labs}
- **Simulating the Hardened DDR Memory Controllers**
  Illustrates how to perform hardened DDR memory controller simulation and describes the creation of test benches. {Lecture, Labs}

Day 2

- **Implementing the Hardened DDR Memory Controllers**
  Demonstrates how to perform DDR memory controller implementation with a brief discussion of the pin planning process. {Lecture, Lab}
- **DDRMC Performance Tuning**
  Discusses quality of service (QoS) and bandwidth aspects and provides a detailed description of performance tuning options. {Lecture, Lab}
- **Debugging the Memory Interfaces**
  Outlines various options to debug memory interfaces. {Lecture, Lab}

- **DDR4 Soft Controller**
  Reviews the basic architecture and functionality of the DDR4 soft controller and describes the traditional design flow for all soft controllers. {Lecture}
- **Memory Interfaces PCB Design**
  Describes board design issues involving signal integrity, the power supply, reference clocking, and trace design. {Lecture}

Register Today

Morgan Advanced Programmable Systems, Inc. (Morgan A.P.S.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota, and Wisconsin.

Visit **morgan-aps.com/training**, for full course schedule and training information.

Morgan Advanced Programmable Systems

- You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

Morgan A.P.S. Course Cancellation Policy

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.

Online or in person training with real hardware

- Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your Xilinx based device quickly and efficiently.