Designing with the Versal Adaptive SoC: Hardware Debug

VER-DEBUG (v1.0)

Course Specification

Course Description

This course describes the tools and techniques available to debug AMD Versal™ devices. You will learn about features for debugging the fabric (programmable logic) and the hard blocks. The course also covers ChipScoPy APIs, which provide a Python™ interface to program and debug the Versal devices.

The emphasis of this course is on:

- Describing the Versal device design flows
- Enumerating the Versal device debug features for programmable logic (PL) and hard block debugging
- Debugging the Versal device using different debug IP cores
- Using ChipScoPy APIs for hardware debugging
- Improving Versal device system performance

What's New for 2025.2

- All labs have been updated to the latest software versions

Level – VER 2

Course Details

- 1 day instructor led training (online or in person)
- 7 lectures
- 3 labs

Price – $800 or 8 AMD Training Credits

Course Part Number – VER-DEBUG

Who Should Attend? – Hardware developers and system architects and anyone who wants to learn about the tools and techniques available to debug the Versal device

Prerequisites

- Designing with the Versal Adaptive SoC: Architecture
- Familiarity with the Vivado™ Design Suite

Subsequent Training

- Designing with the Versal Adaptive SoC: Design Methodology

Software Tools

- Vivado Design Suite 2025.2
- Vitis™ Unified IDE 2025.2

Hardware

- Architecture: Versal adaptive SoC
- Demo board: Versal VCK190 Evaluation Platform

After completing this comprehensive training, you will have the necessary skills to:

- Describe the different tool flows for AMD Versal devices
- Identify the debug interfaces in the Versal devices
- Utilize different debug IP cores, such as the AXIS ILA and AXIS VIO cores
- Identify the different hard block debugging tools
- Describe the Versal device debugging techniques for JTAG low-speed debug and high-speed debug port (HSDP) debug
- Utilize ChipScoPy APIs for hardware debugging

Course Outline

- **Design Tool Flow**

  Maps the various compute resources in the Versal architecture to the tools required and describes how to target them for final image assembly. {Lecture, Lab}
- **Configuration and Debugging**

  Describes the configuration and debug process for the Versal devices, including the Versal device debug interfaces, such as the test access port (TAP) and debug access port (DAP) controller. Also introduces the new PDI debug utility for decoding and analyzing boot configuration errors. {Lecture}
- **Fabric Debug**

  Explains the fabric debug features available in the Versal devices and reviews the different supported debug IP cores, such as the AXI Debug Hub, AXIS ILA, and AXIS VIO. {Lecture, Lab}
- **Hard Block Debug**

  Focuses on the debugging of Versal device hard blocks, such as the GTs, NoC, DDRMC, HBM, PCIe® block, PS, and AI Engines. {Lecture}
- **Overview of HSDP**

  Describes the high-speed debug port (HSDP) in the Versal device. Also goes over the steps to use the SmartLynq+ module for high-speed debugging. {Lecture, Lab}
- **ChipScoPy Overview**

  Discusses the ChipScope hardware debug method and reviews how the ChipScoPy APIs are used for debugging the Versal device. {Lecture}
- **System Integration and Validation Methodology**

  Describes different simulation flows as well as timing and power closure techniques. Also explains how to improve system performance. {Lecture}

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Online or in person training with real hardware

- Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your AMD based device quickly and efficiently.