Designing with the Versal Adaptive SoC: Architecture

VER-ARCH (v1.0)

Course Specification

Course Description

Learn about the AMD Versal™ adaptive SoC architecture building blocks, such as the programmable logic, high-speed I/O, clocking, processing system, AI Engines, and the programmable network on chip (NoC). Also learn how to use leading-edge memory and interfacing technologies to deliver powerful heterogeneous acceleration for any application.

The emphasis of this course is on:

- Reviewing the architecture of the Versal adaptive SoC
- Describing the different compute resources available in the Versal architecture
- Describing the architectures of the network on chip (NoC) and AI Engine
- Outlining the memory solutions and programming interfaces available in the Versal adaptive SoC
- Identifying the PCI Express® and serial transceiver solutions available in the Versal adaptive SoC

What's New for 2025.2

- All labs have been updated to the latest software versions

Level – VER 1

Course Details

- 2 days instructor led training (online or in person)
- 18 lectures
- 8 labs

Price – $1,600 or 16 AMD Training Credits

Course Part Number – VER-ARCH

Who Should Attend? – Software and hardware developers, system architects, DSP users, and anyone who wants to learn about the architecture of the Versal adaptive SoC

Prerequisites

- Basic knowledge of AMD FPGAs and adaptive SoCs
- Basic knowledge of the Vivado™ and Vitis™ tools

Subsequent training

- Designing with the Versal Adaptive SoC: Design Methodology

Software Tools

- Vivado Design Suite 2025.2
- Vitis unified software platform 2025.2

Hardware

- Architecture: Versal adaptive SoC
- Demo board: Versal VCK190 Evaluation Platform or Versal VEK280 Evaluation platform

After completing this comprehensive training, you will have the necessary skills to:

- Describe the AMD Versal adaptive SoC architecture
- Identify the different compute resources available in the Versal devices
- Utilize the hardened blocks available in the Versal architecture
- Describe the NoC and AI Engine architectures
- Outline the memory solutions and programming interfaces available in the Versal adaptive SoC
- Identify the PCI Express and serial transceiver solutions available in the Versal adaptive SoC

Course Outline

Day 1

- **Introduction and Portfolio Overview**
  Describes the need for Versal devices and offers an overview of the Versal portfolio. {Lecture}
- **Architecture Overview**
  Provides a high-level overview of the Versal architecture, illustrating the various compute resources available in the Versal architecture. {Lecture}
- **Design Tool Flow**
  Maps the various compute resources in the Versal architecture to the tools required and describes how to target them for final image assembly. {Lecture, Lab}
- **Programmable Logic (PL)**
  Describes the logic resources available in the programmable logic. {Lecture}
- **SelectIO Resources**
  Describes the I/O bank, SelectIO™ interface, and I/O delay features. {Lecture}
- **Clocking Architecture**
  Discusses the clocking architecture, clock buffers, clock routing, clock management functions, and clock de-skewing options. {Lecture, Lab}
- **Processing System**
  Reviews the Arm® Cortex® APUs and RPUs that form the processing system. The platform management controller (PMC), processing system manager (PSM), I/O peripherals, and PS-PL interfaces are also covered. {Lecture}
- **Platform Management Controller (PMC)**
  Describes the platform management controller architecture and the role of platform loader and manager (PLM) in the Versal device boot process. {Lecture}
- **Boot and Configuration**
  Covers the boot phases, flows, and modes along with the process of generating a boot image. Also discusses the concept and benefits of segmented configuration. {Lecture, Lab}
- **System Interrupts**
  Discusses the different system interrupts and interrupt controllers. {Lecture}

Day 2

- **Timers, Counters, and RTC**
  Provides an overview of timers and counters, including the system counter, triple timer counter (TTC), watchdog timer, and real-time clock (RTC). {Lecture}
- **DSP Engine**
  Describes the DSP58 slice and compares the DSP58 slice with the DSP48 slice. DSP58 modes and applications are also covered in detail. {Lecture, Lab}
- **AI Engine**
  Discusses the AI Engine array architectures (AIE, AIE-ML, and AIE-ML v2), terminology, and AIE interfaces. Also lists the key differences between the AIE, AIE-ML, and AIE-ML v2 architectures. {Lecture, Lab}

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- **NoC Introduction and Concepts**
  Covers the reasons to use the network on chip, its basic elements, design entry flows, and common terminology. {Lecture, Lab}
- **Memory Solutions**
  Describes the available memory resources, such as block RAM, UltraRAM, LUTRAM, embedded memory, OCM, and DDR. The integrated memory controllers are also covered. {Lecture}
- **Programming Interfaces**
  Reviews the various programming interfaces in the Versal device. {Lecture}
- **PCI Express**
  Provides an overview of the PCIe module and describes the PL and CPM PCIe blocks. {Lecture, Lab}
- **Serial Transceivers**
  Describes the transceivers in the Versal device. Also introduces the new GT Wizard Subsystem flow. {Lecture, Lab}

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Morgan Advanced Programmable Systems

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- Student cancellations must be sent here.

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Online or in person training with real hardware

- Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your AMD based device quickly and efficiently.