

Course Description

Are you interested in learning how to effectively utilize Spartan®-6 FPGA architectural resources? This course supports both experienced and less experienced FPGA designers who have already completed the *Essentials of FPGA Design* course. This course focuses on understanding as well as how to properly design for the primary resources found in this popular device family.

Topics covered include device overviews, CLB construction, DCM and PLL clocking resources, global and I/O clocking techniques, memory, DSP, and source-synchronous resources. Memory controller support and the dedicated hardware resources available in each of the sub-families (PCI Express® technology, memory controller block, and GTP transceivers) are also introduced.

This course also includes a detailed discussion about proper HDL coding techniques that enables designers to avoid common mistakes and get the most out of their FPGA. A combination of modules and labs allow for practical hands-on application of the principles taught.

Level – FPGA 3

Course Duration – 2 days

Price – \$1,600 or 16 Xilinx Training Credits

Course Part Number – S6-21000-13-ILT

Who Should Attend? – For those who have taken the *Essentials of FPGA Design* course

Prerequisites

- *Essentials of FPGA Design* course
- Intermediate VHDL or Verilog knowledge

Software Tool

- Xilinx ISE® Design Suite: Logic or System Edition 13.1

Hardware

- Architecture: Spartan-6 FPGA*
- Demo board: None*

* This course focuses on the Spartan-6 and Virtex-6 architectures. Check with [Morgan Advanced Programmable Systems, Inc.](http://www.morgan-aps.com) for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe all the functionality of the 6-input LUT and the CLB construction of the Spartan-6 FPGA
- Specify the CLB resources and the available slice configurations
- Define the block RAM and DSP resources available for the Spartan-6 FPGA
- Properly design for the I/O block and SERDES resources
- Identify the DCM, PLL, and clock routing resources included with this family
- Identify the features and supported memory controllers of the hard memory controller block
- Properly code your HDL to get the most out of the Spartan-6 FPGA
- Describe the additional dedicated hardware for all the Spartan-6 family members

Course Outline

Day 1

- Spartan-6 FPGA Overview
- CLB Architecture
- HDL Coding Techniques
- **Lab 1:** CLB Resources
- Memory Resources

- DSP Resources
- **Lab 2:** DSP Resources
- Basic I/O Resources
- Spartan-6 FPGA I/O Resources

Day 2

- **Lab 3:** I/O Resources
- Basic Clocking Resources
- Spartan-6 FPGA Clocking Resources
- **Lab 4:** Clocking Resources
- Memory Controllers
- Dedicated Hardware

Lab Descriptions

- **Lab 1: CLB Resources** – Using XST, synthesize a 32-bit incrementer with terminal count logic and pipelining registers. Verify that the appropriate resources were used with the RTL and technology viewers included with XST. Use the FPGA Editor to inspect the implemented results.
- **Lab 2: DSP Resources** – Using XST, synthesize and implement a 17x17 MACC. Device usage will be verified via the FPGA Editor. Using the CORE Generator™ tool, construct, instantiate, and implement a wide pipelined multiplier. Verify the results with the FPGA Editor.
- **Lab 3: I/O Resources**– Using the ISE tools, complete the construction of the transmit SERDES datapath. Explore, through simulation, the behavior of the various blocks. Also use the FPGA Editor to explore the physical resources of the Spartan-6 FPGA used for construction of a high-speed interface.
- **Lab 4: Clocking Resources** – Using the Clocking Wizard, build and optimize the appropriate PLL, DCM, and clock routing resources. Also instantiate these resources into the design. After the design is implemented, verify hardware usage with the FPGA Editor and explore other aspects of the silicon layout.

Register Today

Morgan Advanced Programmable Systems, Inc. (MAPS, Inc.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota and Wisconsin.

Visit morgan-aps.com/training, for full course schedule and training information.



You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent [here](http://www.morgan-aps.com/training).

MAPS Inc. Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- MAPS may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is MAPS responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us [here](#).