AI Assisted design of ADC interface for Vivado and Vitis

MPSoC-AI (v1.0)

Course Specification

Course Description

This workshop demonstrates how to drive an AI coding agent through a complete AMD Zynq™ UltraScale+™ MPSoC design — from an empty Vivado™ project to running hardware with a live host display — and, just as importantly, how to review what the agent produces.

The build is a working signal measurement system: an AMD Zynq UltraScale+ device on an Avnet ZUBoard 1CG, a Digilent "Zmod Scope" 1410-105 dual 14-bit ADC, a programmable logic data path that frames the 100 MHz sample stream and runs a 1024-point FFT, and a baremetal application on the Arm® Cortex®-A53 that streams the spectrum to a host over UART.

The emphasis is on where the engineer's judgment remains decisive. During this build the agent produced results that were plausible and wrong three separate times: vendor IP migrated with the wrong device-family primitives, an FFT core generated without a reset pin, and a sample-rate constant hardcoded from an assumption. None of them raised an error. Each was caught by review discipline rather than by the tool.

Level – AMD SoC Design 1

Course Details

Course Duration - 3 hours instructor led training (online or in person)

- 1 lecture
- 1 demonstration

Date – 10-07-2026 (REGISTER HERE)

Pacific: 9:00 AM to 1:00 PM
Mountain: 10:00 AM to 2:00 PM
Central: 11:00 AM to 3:00 PM
Eastern: 12:00 PM to 4:00 PM

Price – Free

Optional – Elect to enroll in drawing for ZUBoard 1CG, an Avnet development card

Course Part Number – MPSoC-AI

Who Should Attend? – FPGA and embedded engineers who want to use AI coding agents in production SoC development without giving up design rigor

Prerequisites

- RTL design experience in VHDL or Verilog
- C programming experience, including general debugging techniques
- Working familiarity with the Vivado IP integrator block design flow
- Conceptual understanding of AXI4-Lite and AXI4-Stream interfaces

Software Tools

- AMD Vivado™ ML Standard Edition
- AMD Vitis™ Unified IDE
- Claude Code (AI coding agent)
- Python 3 with pyserial, NumPy, and Matplotlib

Hardware

- Architecture: Zynq™ UltraScale+™ MPSoC
- Demo board: Avnet ZUBoard 1CG*
- Digilent Zmod Scope 1410-105 — dual 14-bit ADC, 105 MSPS
- Function generator

* This is a demonstration session; the hardware is driven by the instructor. Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the demonstration hardware or a private delivery.

After completing this session, you will be able to:

- Describe how an AI coding agent fits into a Vivado and Vitis™ flow targeting a Zynq UltraScale+ MPSoC, and where it fails
- Structure project context and prompts so generated HDL and software are grounded in vendor documentation
- Recognize the failure modes specific to AI-generated HDL — unconnected resets, wrong device-family primitives, silent configuration errors
- Apply a systematic review checklist — clock domain crossings, reset architecture, AXI compliance, data formats, timing — to AI-generated designs

Course Outline

- **AI-Assisted FPGA Development: What Changes and What Does Not**
  Where an AI coding agent adds leverage in an SoC flow, where it fails, and why the engineer still owns intent and verification.
- **Establishing Project Context for the Agent**
  Capturing target hardware, documentation sources, and goal conditions so the agent works from the correct references instead of plausible assumptions.
- **Project Bring-Up and Vendor IP Migration**
  Creating the Vivado project and base block design, then importing the Zmod Scope controller IP and migrating its 7 series primitives, clocking, and timing constraints to UltraScale+.
- **Building the Measurement Data Path**
  Peak-to-peak detection, stream framing, a 1024-point streaming FFT, magnitude computation, and a DDS signal source for stimulus without external hardware.
- **Reset Architecture, PS Control, and Board Constraints**
  Separating control-plane and datapath reset domains, adding software-controlled acquisition and status readback, and deriving a SYZYGY pinout XDC by cross-checking schematics against the hardware user guide.
- **Baremetal Application and Live Host Display**
  Bring-up and diagnostics on the Cortex-A53, framed UART transport, a Python host application for live spectrum display, and the stacked failure behind it: an unconnected FFT reset, a silently failed ADC configuration, and a self-backpressured stream.
- **Review Methodology for AI-Generated Designs**
  The checklist that separates a demo from a product: clock domain crossings, reset architecture, AXI protocol compliance, signed and unsigned data paths, resource utilization, timing constraints, interrupt handling, and simulation coverage.

Register Today

Morgan Advanced Programmable Systems, Inc. (Morgan A.P.S.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota, and Wisconsin.

Visit **morgan-aps.com/training**, for full course schedule and training information.

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Student Cancellation Policy

- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

Morgan A.P.S. Course Cancellation Policy

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.

Online or in person training with real hardware

- Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your AMD based device quickly and efficiently.

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