

MPSOC-ACAP-SA (v1.0)

Course Description

This course provides system architects with an overview of the capabilities and support for the AMD Zynq[™] UltraScale+[™] MPSoC and Versal[™] adaptive SoC devices.

The emphasis is on:

- Utilizing power management strategies effectively
- Leveraging the platform management unit (PMU) capabilities
- Running the system securely and safely
- Reviewing the high-level architecture of the devices
- Identifying appropriate boot sequences

What's New for 2024.1

- All labs have been updated to the latest software versions
- Labs for PMU: System Power Management and Detecting a Failed Linux Boot labs have been added

Level – Embedded System Architect 3

Course Details

- 2 days live instructor led training (online or in person)
 - 25 lectures
 - 7 labs
 - 5 demos

Price - \$1,600 or 16 AMD Training Credits

Course Part Number – MPSOC-ACAP-SA

Who Should Attend? – System architects interested in understanding the capabilities and ecosystem of the Zynq UltraScale+ MPSoC and Versal adaptive SoC devices.

Prerequisites

- Suggested: Understanding of the Zynq 7000 SoC, Zynq UltraScale+ MPSoC, and/or Versal adaptive SoC architectures
- Familiarity with embedded operating systems

Software Tools

- Vivado[™] Design Suite 2024.1
- Vitis[™] Unified IDE 2024.1
- Hardware emulation environment:
 - VirtualBox (We use faster native installation)
 - QEMU (We use faster hardware)
 - Ubuntu desktop
 - PetaLinux

Hardware

- Zynq UltraScale+ MPSoC ZCU104 board*
- Versal adaptive SoC VCK190 board*

* This course focuses on the Zynq UltraScale+ MPSoC, Zynq 7000 SoC, and Versal adaptive SoC architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab environment or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Effectively use power management strategies and leverage the capabilities of the platform management unit (PMU)
- Identify mechanisms to secure and safely run the system
- Outline the high-level architecture of the devices
- Define the boot sequences appropriate to system requirements

Adaptive SoCs for System Architects

Course Specification

Course Outline

Day 1

Zynq UltraScale+ MPSoC Overview

Overview of the Zynq UltraScale+ MPSoC device. {Lecture, Demo, Lab}

QEMU

Introduction to the Quick Emulator, which is the tool used to run software for the Zynq UltraScale+ MPSoC device when hardware is not available. {Lectures, Demo, Lab}

Safety and Security

Defines what safety and security is in the context of embedded systems and introduces several standards. {Lectures, Demo}

Power Management

Overview of the PMU and the power-saving features of the device. {Lectures, Demo, Lab}

Day 2

System Coherency

Learn how information is synchronized within the API and through the ACE/AXI ports. {Lectures}

DDR and QoS

Understand how DDR can be configured to provide the best performance for your system. {Lectures, Demo, Lab}

Booting

How to implement the embedded system, including the boot process and boot image creation. {Lectures, Labs}

Zynq UltraScale+ MPSoC Ecosystem Support Overview of supported operating systems, software stacks, hypervisors, etc. {Lecture}

Debugging Using Cross-Triggering Illustrates how HW-SW cross-triggering techniques can uncover issues. {Lecture, Lab}

Register Today

Morgan Advanced Programmable Systems, Inc. (Morgan A.P.S.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota, and Wisconsin.

Visit morgan-aps.com/training, for full course schedule and training information.

Morgan

 You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent <u>here</u>.

Morgan A.P.S. Course Cancellation Policy

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AMD together we advance



Advanced Programmable Systems

Adaptive SoCs for System Architects

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Course Specification

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us <u>here</u>.

Online or in person training with real hardware

- Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person...for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your Xilinx based device quickly and efficiently.

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