Verification with SystemVerilog

FPGA 1

LANG-SVVER (v1.0)

Course Specification

Course Description

This course introduces SystemVerilog constructs for verification.

This emphasis is on:

- Writing testbenches to verify a design under test (DUT) utilizing the constructs available in SystemVerilog
- Reviewing object-oriented modeling, data types, reusable tasks and functions, randomization, code coverage, assertions, and the Direct Programming Interface (DPI)

What's New for 2021.1

- All labs have been updated to the latest software versions

Level – FPGA 1

Course Details

- 2 days live instructor led training (online or in person)
- 10 lectures
- 5 labs

Price – $1,600 or 16 Xilinx Training Credits

Course Part Number – LANG-SVVER

Who Should Attend? – Hardware and verification engineers

Prerequisites

- Experienced Verilog user or completion of the Designing with Verilog course

Recommended

- *Designing with SystemVerilog* course

Software Tools

- Vivado® Design Suite 2021.1

Hardware

- Architecture: N/A*
- Demo board: None*

* This course does not focus on any particular architecture. Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the advantages and enhancements to SystemVerilog to support verification
- Define the new data types available in SystemVerilog
- Analyze and use the improvements to tasks and functions
- Discuss and use the various new verification building blocks available in SystemVerilog
- Describe object-oriented programming and create a class-based verification environment
- Explain the various methods for creating random data
- Create and utilize random data for generating stimulus to a DUT
- Identify how SystemVerilog enhances functional coverage for simulation verification
- Utilize assertions to quickly identify correct behavior in simulation
- Identify how the direct programming interface can be used with C/C++ in a verification environment

Course Outline

Day 1

- Introduction to SystemVerilog for Verification
- Data Types
- Tasks and Functions
- **Lab 1:** Implementing Tasks and Functions
- SystemVerilog Verification Building Blocks
- **Lab 2:** Connecting the Testbench to the DUT
- Object-Oriented Modeling
- **Lab 3:** Object-Oriented Modeling

Day 2

- Randomization
- **Lab 4:** Randomization
- Coverage
- **Lab 5:** Coverage
- Assertions
- **Lab 6:** Assertions
- Direct Programming Interface
- **Demo:** Direct Programming Interface
- Inter Process Communication

Lab Descriptions

- **Lab 1:** Implementing Tasks and Functions – Use a task and function to provide input data for a DUT and perform simulation.
- **Lab 2:** Connecting the Testbench to the DUT – Utilize new SystemVerilog verification building blocks to connect the input data to the DUT.
- **Lab 3:** Object-Oriented Modeling – Use object-oriented programming concepts to create a class for enhancing the verification of the DUT.
- **Lab 4:** Randomization – Create random data as input into the DUT to fully validate the design.
- **Lab 5:** Coverage – Create and use a coverage group to validate the code coverage for the DUT. Adjust and revalidate the coverage.
- **Lab 6:** Assertions – Create an assertion to validate all possible conditions are verified for the DUT.

Register Today

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Visit **morgan-aps.com/training**, for full course schedule and training information.

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.

- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

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- We regret from time-to-time classes will need to be rescheduled or cancelled.
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- For additional information or to schedule a private class contact us here.

Online training with real hardware

During the Covid-19 period, some companies do not allow their staff to participate in live in-person training.

- Consequently, Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your Xilinx based device quickly and efficiently.