Designing with SystemVerilog

FPGA 1

LANG-SVDES (v1.0)

Course Specification

Course Description

This course provides a thorough introduction to SystemVerilog constructs for design.

This focus is on:

- Writing RTL code using the new constructs available in SystemVerilog
- Reviewing new data types, structs, unions, arrays, procedural blocks, re-usable tasks, functions, and packages
- Targeting and optimizing Xilinx devices using SystemVerilog

What's New for 2021.1

- All labs have been updated to the latest software versions

Level – FPGA 1

Course Details

- 2 days
- 16 lectures
- 6 labs

Price – $1,600 or 16 Xilinx Training Credits

Course Part Number – LANG-SVDES

Who Should Attend? – FPGA designers and logic designers

Prerequisites

- Verilog design experience or completion of Designing with Verilog

Software Tools

- Vivado® Design Suite 2021.1
- Questa Sim Prime Simulator 2019.4

Hardware

- Architecture: N/A*
- Demo board: Kintex® UltraScale™ FPGA KCU105 board*

* This course does not focus on any particular architecture. Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the features and benefits of using SystemVerilog for RTL design
- Identify the new data types supported in SystemVerilog
- Use an enumerated data type for coding a finite state machine (FSM)
- Explain how to use structures, unions, and arrays
- Describe the new procedural blocks and analyze the affected synthesis results
- Define the enhancements and ability to reuse tasks, functions, and packages
- Identify how to simplify module definitions and instantiations using interfaces
- Examine how to efficiently code in SystemVerilog for FPGA design simulation and synthesis
- Target and optimize Xilinx FPGAs by using SystemVerilog
- Synthesize and analyze SystemVerilog designs with the Vivado Design Suite
- Download a complete SystemVerilog design to an evaluation board

Course Outline

Day 1

- **Introduction to SystemVerilog**
  Introduces the SystemVerilog language. {Lecture}
- **Data Types**
  Describes the data types supported by SystemVerilog. {Lecture, Lab, Demo}
- **User-Defined and Enumerated Data Types**
  Describes user-defined and enumerated data types supported by SystemVerilog. {Lecture}
- **Type Casting**
  Describes type casting in SystemVerilog. {Lecture}
- **Arrays and Strings**
  Explains the use of arrays in SystemVerilog. {Lecture}
- **SystemVerilog Building Blocks**
  Describes the design and verification building blocks in SystemVerilog. {Lecture}
- **Structures**
  Explains the use of structures in SystemVerilog. {Lecture, Lab}
- **Unions**
  Explains the use of unions in SystemVerilog. {Lecture, Lab}
- **Additional Operators in SystemVerilog**
  Describes the operators supported by SystemVerilog beyond those found in Verilog. {Lecture}

Day 2

- **Procedural Statements**
  Describes the different procedural blocks provided by SystemVerilog. {Lecture, Lab}
- **Control Flow Statements**
  Describes the different control statements provided by SystemVerilog. {Lecture}
- **Functions**
  Explains the SystemVerilog enhancements to functions. {Lecture}
- **Tasks**
  Describes the task SystemVerilog construct. {Lecture}
- **Packages**
  Describes the package SystemVerilog construct. {Lecture, Lab}
- **Interfaces**
  Describes the concept of interfaces in SystemVerilog. {Lecture}
- **Targeting Xilinx FPGAs**
  Focuses on Xilinx-specific implementation and chip-level optimization. {Lecture, Lab}

Register Today

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Visit **morgan-aps.com/training**, for full course schedule and training information.

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

Morgan A.P.S. Course Cancellation Policy

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.

Online training with real hardware

During the Covid-19 period, some companies do not allow their staff to participate in live in-person training.

- Consequently, Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your Xilinx based device quickly and efficiently.