Designing with SystemVerilog

FPGA 1

LANG-SVDES-ILT (v1.0)

Course Specification

Course Description

This comprehensive course is a thorough introduction to SystemVerilog constructs for design. This class addresses writing RTL code using the new constructs available in SystemVerilog. New data types, structs, unions, arrays, procedural blocks, re-usable tasks, functions, and packages are all covered. The information gained can be applied to any digital design. This course combines insightful lectures with practical lab exercises to reinforce key concepts.

In this two-day course, you will gain valuable hands-on experience. Incoming students with a Verilog background will finish this course empowered with the ability to more efficiently develop RTL designs.

Level – FPGA 1
Course Duration – 2 days
Price – $1,600 or 16 Xilinx Training Credits
Course Part Number – LANG-SVDES-ILT
Who Should Attend? – FPGA designers and logic designers
Prerequisites

- Verilog design experience or completion of *Designing with Verilog*

Software Tools

- Vivado® Design or System Edition 2018.1
- Questa Sim Prime Simulator 10.6c

Hardware

- Architecture: N/A*
- Demo board: Kintex® UltraScale™ FPGA KCU105 board or Kintex-7 FPGA KC705 board*

* This course does not focus on any particular architecture.

** Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the features and benefits of using SystemVerilog for RTL design
- Identify the new data types supported in SystemVerilog
- Use an enumerated data type for coding a finite state machine (FSM)
- Explain how to use structures, unions, and arrays
- Describe the new procedural blocks and analyze the affected synthesis results
- Define the enhancements and ability to reuse tasks, functions, and packages
- Identify how to simplify module definitions and instantiations using interfaces
- Examine how to efficiently code in SystemVerilog for FPGA design simulation and synthesis
- Target and optimize Xilinx FPGAs by using SystemVerilog
- Synthesize and analyze SystemVerilog designs with the Vivado Design Suite
- Download a complete SystemVerilog design to an evaluation board

Course Outline

Day 1

- Introduction to SystemVerilog {Lecture}
- Data Types {Lecture, Lab, Demo}
- User-Defined and Enumerated Data Types {Lecture}
- Type Casting {Lecture}
- Arrays and Strings {Lecture}
- SystemVerilog Building Blocks {Lecture}
- Structures {Lecture, Lab}
- Unions {Lecture, Lab}
- Additional Operators in SystemVerilog {Lecture}

Day 2

- Procedural Statements {Lecture, Lab}
- Control Flow Statements {Lecture}
- Functions {Lecture}
- Tasks {Lecture}
- Packages {Lecture, Lab}
- Interfaces {Lecture}
- Targeting Xilinx FPGAs {Lecture, Lab}

Topic Descriptions

Day 1

- Introduction to SystemVerilog – Provides an introduction to the SystemVerilog language.
- Data Types – Describes the data types supported by SystemVerilog.
- User-Defined and Enumerated Data Types – Describes user-defined and enumerated data types supported by SystemVerilog.
- Type Casting – Describes type casting in SystemVerilog.
- Arrays and Strings – Explains the use of arrays in SystemVerilog.
- SystemVerilog Building Blocks – Describes the design and verification building blocks in SystemVerilog.
- Structures – Explains the use of structures in SystemVerilog.
- Unions – Explains the use of unions in SystemVerilog.
- Additional Operators in SystemVerilog – Describes the operators supported by SystemVerilog beyond those found in Verilog.

Day 2

- Procedural Statements – Describes the different procedural blocks provided by SystemVerilog.
- Control Flow Statements – Describes the different control statements provided by SystemVerilog.
- Functions – Explains the SystemVerilog enhancements to functions.
- Tasks – Describes the task SystemVerilog construct.
- Packages – Describes the package SystemVerilog construct.
- Interfaces – Describes the concept of interfaces in SystemVerilog.
- Targeting Xilinx FPGAs – Focuses on Xilinx-specific implementation and chip-level optimization.

Register Today

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

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