

Course Description

This course provides hardware and firmware engineers with the knowledge to effectively utilize a Zynq® System on a Chip (SoC). It covers the architecture of the ARM® Cortex™-A9 processor-based processing system (PS) and the integration of programmable logic (PL).

The course details the individual components that comprise the PS: I/O peripherals, timers, caching, DMA, interrupt, and memory controllers. Emphasis is placed on effective access and usage of the PS DDR controller from PL user logic, efficient PL-to-PS interfacing, and design techniques, tradeoffs, and advantages of implementing functions in the PS or the PL.

Level – Embedded Hardware and Firmware 3

Course Duration – 1 day

Price – \$800 or 8 Xilinx Training Credits

Course Part Number – INTRO-ZARCH-ILT

Who Should Attend? – Hardware and firmware engineers who are interested in implementing a system on a chip using the Zynq SoC and programmable logic.

Prerequisites

- FPGA design experience
- Completion of the *Designing FPGAs Using the Vivado Design Suite 1* course or equivalent knowledge of the Vivado® Design Suite implementation tools
- Basic understanding of C programming
- Basic understanding of microprocessors
- Some HDL modeling experience

Software Tools

- Vivado® Design or System Edition 2018.1

Hardware

- Architecture: Zynq-7000 SoC*
- Demo board: Zynq-7000 SoC ZC702 or ZedBoard*

* This course focuses on the Zynq-7000 SoC.

** Check with [Morgan Advanced Programmable Systems, Inc.](http://www.morgan-aps.com) for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the architecture and components that comprise the Zynq SoC processing system (PS)
- Evaluate a processing system (PS) and programmable logic (PL) AXI interface
- Identify the boot options for the Zynq SoC

Course Outline

- Overview {Lecture, Demo}
- Application Processor Unit (APU) {Lecture, Lab}
- Processor Input/Output Peripherals {Lecture, Demo}
- PS-PL Interface {Lecture, Demo, Lab}
- Booting {Lecture, Lab}
- Memory Resources {Lecture, Demo}

Topic Descriptions

- Overview – Provides a general overview of the Zynq SoC.
- Application Processor Unit (APU) – Explores the individual components that comprise the APU.
- Processor Input/Output Peripherals – Introduces the components that comprise the IOP block of the Zynq device PS.
- PS-PL Interface – Describes in detail the PS interconnect and how it affects PL architecture decisions.
- Booting – Explains the boot process of the PC and configuration of the PL.
- Memory Resources – Explains the operation of the on-chip (OCM) memory and various memory controllers located in the PS.

Register Today

Morgan Advanced Programmable Systems, Inc. (MAPS, Inc.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota and Wisconsin.

Visit morgan-aps.com/training, for full course schedule and training information.



You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent [here](#).

MAPS Inc. Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- MAPS may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is MAPS responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
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