

## Course Description

This course provides hardware and firmware engineers with the knowledge on how to best architect a Zynq® System on a Chip (SoC) device project.

This course covers:

- Describing the architecture of the ARM® Cortex™-A9 processor-based processing system (PS) and the integration of programmable logic (PL)
- Detailing the individual components that comprise the PS: I/O peripherals, timers, caching, DMA, interrupt, and memory controllers
- Effectively accessing and using the PS DDR controller from PL user logic
- Interfacing PL-to-PS efficiently
- Employing best practice design techniques for implementing functions in the PS or PL

**Level** – Embedded Hardware and Firmware 3

### Course Details

- 1 day live instructor led training (online or in person)
- 6 lectures
- 3 labs
- 4 demos

**Price** – \$800 or 8 Xilinx Training Credits

**Course Part Number** – INTRO-ZARCH

**Who Should Attend?** – Hardware and firmware engineers who are interested in implementing a system on a chip using the Zynq SoC and programmable logic.

### Prerequisites

- FPGA design experience
- Completion of the [Designing FPGAs Using the Vivado Design Suite 1](#) course or equivalent knowledge of the Vivado® Design Suite implementation tools
- Basic understanding of C programming
- Basic understanding of microprocessors
- Some [Verilog](#) or [VHDL](#) modeling experience

### Software Tools

- Vivado® Design Suite 2020.1
- Vitis™ unified software platform 2020.1

### Hardware

- Architecture: Zynq-7000 SoC\*
- Demo board: Zynq-7000 SoC ZC702 or ZedBoard\*

\* This course focuses on the Zynq-7000 SoC. Check with [Morgan Advanced Programmable Systems, Inc.](#) for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the architecture and components that comprise the Zynq SoC processing system (PS)
- Evaluate a processing system (PS) and programmable logic (PL) AXI interface
- Identify the boot options for the Zynq SoC

## Course Outline

- Overview**  
Provides a general overview of the Zynq SoC. {Demo}
- Application Processor Unit (APU)**  
Explores the individual components that comprise the APU. {Lab}
- Input/Output Peripherals**  
Introduces the components that comprise the IOP block of the Zynq device PS. {Demo}
- PS-PL Interface**  
Describes in detail the PS interconnect and how it affects PL architecture decisions. {Demo, Lab}
- Memory Resources**  
Explains the operation of the on-chip (OCM) memory and various memory controllers located in the PS. {Demo}
- Bootling**  
Explains the boot process of the PC and configuration of the PL. {Lab}

## Register Today

Morgan Advanced Programmable Systems, Inc. (Morgan A.P.S.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota, and Wisconsin.

Visit [morgan-aps.com/training](http://morgan-aps.com/training), for full course schedule and training information.



You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

## Student Cancellation Policy

- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent [here](#).

## Morgan A.P.S. Course Cancellation Policy

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us [here](#).

## Online training with real hardware

During the Covid-19 period, some companies do not allow their staff to participate in live in-person training.



## Introduction to the Zynq SoC Architecture

Embedded Hardware and Firmware 3

INTRO-ZARCH (v1.0)

### Course Specification

- Consequently, Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person...for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly as planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your Xilinx based device quickly and efficiently.