UltraFast Design Methodology

FPGA 3

FPGA-VDM-ILT (v1.0)

Course Specification

Course Description

This course describes the FPGA design best practices and skills to be successful using the Vivado® Design Suite. This includes the necessary skills to improve design speed and reliability, including: system reset design, synchronization circuits, optimum HDL coding techniques, and timing closure techniques using the Vivado software. This course encapsulates this information with an UltraFast™ design methodology case study. The UltraFast design methodology checklist is also introduced.

Level – FPGA 3

Course Duration – 2 days

Price – $1,600 or 16 Xilinx Training Credits

Course Part Number – FPGA-VDM-ILT

Who Should Attend? – Engineers who seek training for FPGA design best practices that increase design performance and increase development productivity.

Prerequisites

- Basic HDL knowledge (VHDL or Verilog)
- Digital design knowledge and experience
- Vivado Design Suite experience or completion of either:
  - *Designing FPGAs Using the Vivado Design Suite 1* course and
  - *Designing FPGAs Using the* Vivado Design Suite 2 course and
  - *Designing FPGAs Using the Vivado Design Suite 3* course or
  - *Vivado Design Suite Advanced XDC and Static Timing Analysis for ISE Software Users* course

Software Tools

- Vivado Design or System Edition 2018.1

Hardware

- Architecture: UltraScale™ and 7 series FPGAs*
- Demo board: None*

* This course focuses on the UltraScale and 7 series architectures.

** Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the UltraFast™ design methodology checklist
- Identify key areas to optimize your design to meet your design goals and performance objectives
- Define a properly constrained design
- Optimize HDL code to maximize the FPGA resources that are inferred and meet your performance goals
- Build resets into your system for optimum reliability and design speed
- Build a more reliable design that is less vulnerable to metastability problems and requires less design debugging later in the development cycle
- Identify timing closure techniques using the Vivado Design Suite
- Describe how the UltraFast design methodology techniques work effectively through case studies and lab experience

Course Outline

Day 1

- UltraFast Design Methodology: Introduction {Lecture, Demo}
- UltraFast Design Methodology: Board and Device Planning {Lecture}
- Vivado Design Suite I/O Pin Planning {Lecture, Lab}
- Xilinx Power Estimator Spreadsheet {Lecture, Lab}
- Introduction to FPGA Configuration {Lecture}
- UltraFast Design Methodology: Design Creation {Lecture}
- HDL Coding Techniques {Lecture}
- Resets {Lecture, Lab}
- Register Duplication {Lecture}
- Pipelining {Lecture, Lab}
- Synchronous Design Techniques {Lecture}
- Creating and Packaging Custom IP {Lecture}

Day 2

- Designing with the IP Integrator {Lecture, Lab}
- Revision Control Systems in the Vivado Design Suite {Lecture}
- UltraFast Design Methodology: Implementation {Lecture}
- Synthesis and Implementation {Lecture}
- Incremental Compile Flow {Lecture}
- UltraFast Design Methodology: Design Closure {Lecture}
- Introduction to Vivado Reports {Lecture, Demo}
- Baselining {Lecture, Lab}
- Introduction to Timing Exceptions {Lecture, Demo}
- Synchronization Circuits {Lecture}
- Introduction to Floorplanning {Lecture}
- Congestion {Lecture}
- Physical Optimization {Lecture, Lab}
- Power Management Techniques {Lecture}
- Vivado Design Suite Debug Methodology {Lecture}

Topic Descriptions

Day 1

- UltraFast Design Methodology: Introduction – Introduces the UltraFast Design Methodology and the UltraFast Design Methodology checklist.
- UltraFast Design Methodology: Board and Device Planning – Introduces the methodology guidelines on board and device planning.
- Vivado Design Suite I/O Pin Planning – Use the I/O Pin Planning layout to perform pin assignments in a design.
- Xilinx Power Estimator Spreadsheet – Estimate the amount of resources and default activity rates for a design and evaluate the estimated power calculated by XPE.
- Introduction to FPGA Configuration – Describes how FPGAs can be configured.
- UltraFast Design Methodology: Design Creation - Introduces the UltraFast methodology guidelines on design creation.
- HDL Coding Techniques – Covers basic digital coding guidelines used in an FPGA design.
- Resets – Investigates the impact of using asynchronous resets in a design.
- Register Duplication – Use register duplication to reduce high fanout nets in a design.
- Pipelining - Use pipelining to improve design performance.
- Synchronous Design Techniques – Introduces synchronous design techniques used in an FPGA design.
- Creating and Packaging Custom IP – Create your own IP and package and include it in the Vivado IP catalog.

Day 2

- Designing with the IP Integrator – Use the Vivado IP integrator to create the uart_led subsystem.
- Revision Control Systems in the Vivado Design Suite – Use version control systems with Vivado design flows.
- UltraFast Design Methodology: Implementation - Introduces the methodology guidelines on implementation.

- Synthesis and Implementation – Create timing constraints according to the design scenario and synthesize and implement the design. Optionally, generate and download the bitstream to the demo board.
- Incremental Compile Flow – Utilize the incremental compile flow when making last-minute RTL changes.
- UltraFast Design Methodology: Design Closure - Introduces the UltraFast methodology guidelines on design closure.
- Introduction to Vivado Reports – Generate and use Vivado reports to analyze failed paths.
- Baselining – Use Xilinx-recommended baselining procedures to progressively meet timing closure.
- Introduction to Timing Exceptions – Introduces timing exception constraints and applying them to fine tune design timing.
- Synchronization Circuits – Use synchronization circuits for clock domain crossings.
- Introduction to Floorplanning – Introduction to floorplanning and how to use Pblocks while floorplanning.
- Congestion - Identifies congestion and addresses congestion issues.
- Physical Optimization – Use physical optimization techniques for timing closure.
- Power Management Techniques – Identify techniques used for low power design.
- Vivado Design Suite Debug Methodology – Understand and follow the debug core recommendations. Employ the debug methodology for debugging a design using the Vivado logic analyzer.

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

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