UltraFast Design Methodology

FPGA-VDM (v1.0)

Course Specification

Course Description

Learn how to improve design speed and reliability by using the UltraFast™ Design Methodology and the Vivado® Design Suite.

The focus is on:

- Optimizing system reset design and synchronization circuits
- Employing best practice HDL coding techniques
- Applying appropriate timing closure techniques
- Reviewing an UltraFast Design Methodology case study

What's New for 2022.2

- Added content to the following modules:
  - RTL Development, QoR Reports Overview
- All labs have been updated to the latest software versions

Level – FPGA 3

Course Details

- 2 days live instructor led training (online or in person)
- 24 lectures
- 8 labs
- 2 demos

Price – $1,600 or 16 Xilinx Training Credits

Course Part Number – FPGA-VDM

Who Should Attend? – Engineers who seek training for FPGA design best practices that increase design performance and increase development productivity.

Prerequisites

- Basic HDL knowledge (VHDL or Verilog)
- Digital design knowledge and experience

Software Tools

- Vivado Design Suite 2022.2

Hardware

- Architecture: UltraScale™ FPGAs*
- Demo board: None*

* This course focuses on the UltraScale architecture.

Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the UltraFast design methodology checklist
- Identify key areas to optimize your design to meet your design goals and performance objectives
- Define a properly constrained design
- Optimize HDL code to maximize the FPGA resources that are inferred and meet your performance goals
- Build resets into your system for optimum reliability and design speed
- Build a more reliable design that is less vulnerable to metastability problems and requires less design debugging later in the development cycle
- Identify timing closure techniques using the Vivado Design Suite
- Describe how the UltraFast design methodology techniques work effectively through case studies and lab experience

Course Outline

Day 1

UltraFast Design Methodology – Planning

- **UltraFast Design Methodology: Introduction**
  Introduces the UltraFast Design Methodology and the UltraFast Design Methodology checklist. {Lecture, Demo}
- **UltraFast Design Methodology: Board and Device Planning**
  Introduces the methodology guidelines on board and device planning. {Lecture}
- **Vivado Design Suite I/O Pin Planning**
  Describes the I/O Pin Planning layout for performing pin assignments in a design. {Lecture, Lab}
- **Power Estimation Using XPE**
  Illustrates estimating the number of resources and default activity rates for a design and evaluating the estimated power calculated by XPE. {Lecture, Lab}

UltraFast Design Methodology – Design Creation

- **UltraFast Design Methodology: Design Creation**
  Introduces the UltraFast methodology guidelines on design creation. {Lecture}
- **RTL Development**
  Covers RTL and the RTL design flow, recommended coding guidelines, using control signals, and recommendations on resets. {Lecture}
- **Resets**
  Investigates the impact of using asynchronous resets in a design. {Lecture, Lab}
- **Pipelining**
  Demonstrates the use of pipelining to improve design performance. {Lecture, Lab}
- **Synchronous Design Techniques**
  Introduces the synchronous design techniques used in an FPGA design. {Lecture}

Vivado IP Flow

- **Designing with the IP Integrator**
  Demonstrates how to use the Vivado IP integrator to create the uart_led subsystem. {Lecture, Lab}
- **Creating and Packaging Custom IP**
  Covers creating your own IP and package and including it in the Vivado IP catalog. {Lecture}

Version Control Systems

- **Revision Control Systems in the Vivado Design Suite**
  Reviews using version control systems with Vivado IDE design flows. {Lecture}

Day 2

UltraFast Design Methodology – Implementation

- **UltraFast Design Methodology: Implementation**
  Introduces the methodology guidelines on implementation. {Lecture}
- **Incremental Compile Flow**
  Discusses the incremental compile flow last-minute RTL changes are made. {Lecture}

UltraFast Design Methodology – Design Analysis

- **UltraFast Design Methodology Design Closure**
  Introduces the UltraFast methodology guidelines on design closure. {Lecture}

- **Introduction to Vivado Reports**
  Demonstrates generating and using Vivado timing reports to analyze failed timing paths. {Lecture, Demo}
- **Baselining**
  Illustrates how to apply recommended baselining procedures to progressively meet timing closure. {Lecture, Lab}
- **Clock Domain Crossing and Synchronization Circuits**
  Outlines using synchronization circuits for clock domain crossings. {Lecture}
- **QoR Reports Overview**
  Describes what quality of result (QoR) is and how to analyze the QoR reports generated by the Vivado IDE. {Lecture, Lab}
- **Timing Closure Using Physical Optimization Techniques**
  Show how to use physical optimization techniques for timing closure. {Lecture, Lab}
- **Power Management Techniques**
  Identifies the techniques used for low power design. {Lecture}

Floorplanning

- **Introduction to Floorplanning**
  Introduces floorplanning and how to use Pblocks while floorplanning. {Lecture}
- **Congestion**
  Describes congestion and addresses congestion issues. {Lecture}

Debugging

- **Vivado Design Suite Debug Methodology**
  Covers debug core recommendations and employing the debug methodology for debugging a design using the Vivado logic analyzer. {Lecture}

Register Today

Morgan Advanced Programmable Systems, Inc. (Morgan A.P.S.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota, and Wisconsin.

Visit **morgan-aps.com/training**, for full course schedule and training information.

Morgan
Advanced Programmable Systems

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

Morgan A.P.S. Course Cancellation Policy

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.

Online training with real hardware

During the Covid-19 period, some companies do not allow their staff to participate in live in-person training.

- Consequently, Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your Xilinx based device quickly and efficiently.