Designing FPGAs Using the Vivado Design Suite 3

FPGA-VDES3 (v1.0)

Course Specification

Course Description

Learn how to effectively employ timing closure techniques.

This course includes:

- Demonstrating timing closure techniques such as baselining, pipelining, and synchronization circuits
- Showing optimum HDL coding techniques that help with design timing closure
- Illustrating the advanced capabilities of the Vivado® logic analyzer to debug a design

This course builds further on the previous *Designing FPGAs Using the Vivado Design Suite* courses.

What's New for 2022.2

- All labs have been updated to the latest software versions

Level – FPGA 3

Course Details

- 2 days live instructor led training (online or in person)
- 21 lectures
- 14 labs
- 4 demos

Price – $1,600 or 16 Xilinx Training Credits

Course Part Number – FPGA-VDES3

Who Should Attend? – FPGA designers with intermediate knowledge of HDL and FPGA architecture and some experience with the Vivado Design Suite

Prerequisites

- Intermediate HDL knowledge (VHDL or Verilog)
- Solid digital design background
- Designing FPGAs Using the Vivado Design Suite 1 course (recommended)
- Designing FPGAs Using the Vivado Design Suite 2 course (recommended)

Subsequent Courses

- Designing FPGAs Using the Vivado Design Suite 4

Alternative Course

- Vivado Static Timing Analysis, Xilinx Design Constraints, and Advanced Techniques of the Vivado Design Suite training

Optional Videos

- Basic HDL Coding Techniques*
- Power Estimation*

Software Tools

- Vivado Design Suite 2022.2

Hardware

- Architecture: UltraScale™ FPGAs and Versal® ACAPs**
- Demo board: Zynq® UltraScale+™ ZCU104 board

* Go to www.xilinx.com/training and click the Online Training tab to view these videos.

** This course focuses on the UltraScale and Versal architectures. Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Employ good alternative design practices to improve design reliability
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- Define a properly constrained design
- Apply baseline constraints to determine if internal timing paths meet design timing objectives
- Apply appropriate I/O timing constraints and design modifications for source-synchronous and system-synchronous interfaces
- Optimize HDL code to maximize the FPGA resources that are inferred and meet performance goals
- Build a more reliable design that is less vulnerable to metastability problems and requires less design debugging later in the development cycle
- Perform quality of results (QoR) assessments at different stages to improve the QoR score
- Increase performance by utilizing FPGA design techniques
- Use Vivado Design Suite reports and utilities to full advantage, especially the Clock Interaction report
- Describe how to enable remote debug

Course Outline

Day 1

UltraFast Design Methodology (UFDM)

- **UltraFast Design Methodology: Implementation**
  Introduces the methodology guidelines covered in this course. {Lecture}

Simulation

- **Timing Simulation**
  Illustrates simulating a design post-implementation to verify that the design works properly on hardware. {Lecture, Lab}

Design Techniques

- **Baselining**
  Demonstrates how to use recommended baselining procedures to progressively meet timing closure. {Lecture, Demo, Lab}
- **Pipelining**
  Describes using pipelining to improve design performance. {Lecture, Lab}
- **Inference**
  Outlines how to infer AMD Xilinx-dedicated hardware resources by writing appropriate HDL code. {Lecture, Lab}

Timing – Advanced

- **I/O Timing Scenarios**
  Provides an overview of various I/O timing scenarios, such as source- and system-synchronous, direct/MMCM capture, and edge/center-aligned data. {Lecture}
- **System-Synchronous I/O Timing**
  Demonstrates applying I/O delay constraints and performing static timing analysis for a system-synchronous input interface. {Lecture, Demo}
- **Source-Synchronous I/O Timing**
  Demonstrates applying I/O delay constraints and performing static timing analysis for a source-synchronous, double data rate (DDR) interface. {Lecture, Lab}
- **Timing Constraints Priority**
  Reviews how to identify the priority of timing constraints. {Lecture}

Day 2

Design Analysis

- **Report Clock Interaction**
  Describes the clock interaction report, which is used to identify interactions between clock domains. {Lecture, Demo}
- **Report Datasheet**
  Describes the datasheet report, which is used to find the optimal setup and hold margin for an I/O interface. {Lecture, Demo}
- **QoR Reports Overview**
  Discusses what quality of result (QoR) is and how to analyze the QoR reports generated by the Vivado IDE. {Lecture}

CDC

- **Sampling and Capturing Data in Multiple Clock Domains**
  Provides an overview of debugging a design with multiple clock domains that require multiple ILAs. {Lecture, Lab}
- **Clock Domain Crossing (CDC) and Synchronization Circuits**
  Highlights how to use synchronization circuits for clock domain crossings. {Lecture, Lab, Case Study}

Version Control System

- **Revision Control Systems in the Vivado Design Suite**
  Investigates using version control systems with the Vivado design flows. {Lecture, Lab}

Power

- **Dynamic Power Estimation Using Vivado Report Power**
  Describes how to use a SAIF (switching activity interface format) file to determine accurate power consumption for a design. {Lecture, Lab}
- **Versal ACAP: Power and Thermal Solutions**
  Discusses the power domains in the Versal ACAP as well as power optimization and analysis techniques. Thermal design challenges are also covered. {Lecture}

Configuration

- **Configuration Modes**
  Reviews the various configuration modes and selects a suitable mode for a design. {Lecture}

Debugging

- **Netlist Insertion Debug Probing Flow**
  Covers the netlist insertion flow for debugging using the Vivado logic analyzer. {Lecture, Lab}
- **JTAG to AXI Master Core**
  Describes how this debug core is used to write/read data to/from a peripheral connected to an AXI interface in a system that is running in hardware. {Lecture, Demo}
- **Debug Flow in an IP Integrator Block Design**
  Shows how to insert the debug cores into IP integrator block designs. {Lecture, Lab}
- **Remote Debugging Using the Vivado Logic Analyzer**
  Demonstrates using the Vivado logic analyzer to configure an FPGA, set up triggering, and view sampled data from a remote location. {Lecture, Lab}

Tcl Commands

- **Design Analysis Using Tcl Commands**
  Describes how to analyze a design using Tcl commands. {Lecture, Demo}

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Visit **morgan-aps.com/training**, for full course schedule and training information.

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

Morgan A.P.S. Course Cancellation Policy

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.

Online training with real hardware

During the Covid-19 period, some companies do not allow their staff to participate in live in-person training.

- Consequently, Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your Xilinx based device quickly and efficiently.