Designing FPGAs Using the Vivado Design Suite 2

FPGA-VDES2 (v1.0)

Course Specification

Course Description

Learn how to build a more effective FPGA design:

The focus is on:

- Using synchronous design techniques
- Utilizing the Vivado® IP integrator to create a sub-system
- Employing proper HDL coding techniques to improve design performance
- Debugging a design with multiple clock domains

This course builds on the concepts from the *Designing FPGAs Using the Vivado Design Suite 1* course.

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What's New for 2022.2

- Added content on using Tcl commands in the Vivado Design Suite project flow
- All labs have been updated to the latest software versions

Level – FPGA 2

Course Details

- 2 days live instructor led training (online or in person)
- 28 lectures
- 11 labs
- 7 demos

Price – $1,600 or 16 Xilinx Training Credits

Course Part Number – FPGA-VDES2

Who Should Attend? – Digital designers who have a working knowledge of HDL (VHDL or Verilog) and who are new to Xilinx FPGAs

Prerequisites

- Intermediate HDL knowledge (VHDL or Verilog)
- Digital design knowledge and experience (attendees should be electrical engineers)
- Experience with the basics of the Tcl language
- Designing FPGAs Using the Vivado Design Suite 1 (recommended)

Optional Videos

- Basic HDL Coding Techniques*

Software Tools

- Vivado Design Suite 2022.1

Hardware

- Architecture: UltraScale™ FPGAs and Versal® ACAPs*
- Demo board (optional): Zynq® UltraScale+™ MPSoC ZCU104 board*

* Go to www.xilinx.com/training and click the Online Training tab to view this video.

** This course focuses on the UltraScale and Versal architectures. Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Identify synchronous design techniques
- Build resets into your system for optimum reliability and design speed
- Create a Tcl script to create a project, add sources, and implement a design
- Describe and use the clock resources in a design
- Create and package your own IP and add to the Vivado IP catalog to reuse
- Use the Vivado IP integrator to create a block design
- Describe the Versal ACAP clocking architecture and hardware platform development using Vivado IP integrator
- Apply timing exception constraints in a design as part of the Baselining procedure to fine tune the design
- Describe how power analysis and optimization is performed
- Describe the HDL instantiation flow of the Vivado logic analyzer

Course Outline

Day 1

UltraFast Design Methodology

- **UltraFast Design Methodology: Design Creation**
  Introduces the UltraFast methodology guidelines on design creation. {Lecture}

Design Techniques

- **Synchronous Design Techniques**
  Introduces the synchronous design techniques used in an FPGA design. {Lecture}
- **Resets**
  Investigates the impact of using asynchronous resets in a design. {Lecture, Lab}
- **Register Duplication**
  Covers the use of register duplication to reduce high fanout nets in a design. {Lecture}
- **Using Tcl Commands in the Vivado Design Suite Project Flow**
  Introduces basic Tcl commands and executing a Tcl script. {Lecture, Lab}

Clocking in the UltraScale Architecture

- **Clock Structure and Layout in the UltraScale Architecture**
  Describes UltraScale clocking architecture and differences in the clocking architectures between 7 series and UltraScale FPGAs. {Lecture}
- **Clock Buffers in the UltraScale Architecture**
  Reviews the different clock buffers and clock migration. {Lecture}
- **Clock Management in the UltraScale Architecture**
  Highlights clock management resources. {Lecture}
- **Clock Routing in the UltraScale Architecture**
  Describes clock routing, distribution, and the benefits of clock routing. {Lecture, Lab}

I/O in the UltraScale Architecture

- **UltraScale Architecture I/O Resources: Overview**
  Provides an overview of the I/O resources and I/O banks available the UltraScale architecture. {Lecture}
- **UltraScale Architecture I/O Resources: Component Mode**
  Describes component mode, SelectIO™ interface logic, SERDES technology, and programmable delay lines. {Lecture}
- **UltraScale Architecture I/O Resources: Native Mode**
  Describes SelectIO interface logic, BITSLICE technology, native mode clocking, and the High Speed SelectIO Wizard. {Lecture}

IP Integrator

- **Designing with the IP Integrator**
  Demonstrates how to use the Vivado IP integrator to create the uart_led subsystem. {Lecture, Demo, Lab}

- **Block Design Containers in the Vivado IP Integrator**
  Describes the block design container (BDC) feature and shows how to create a BDC in the IP integrator. {Lecture}
- **Creating and Packaging Custom IP**
  Covers creating your own IP and package and including it in the Vivado IP catalog. {Lecture, Lab}
- **Using an IP Container**
  Illustrates how to use a core container file as a single file representation for an IP. {Lecture, Demo}
- **Versal ACAP: Hardware Platform Development Using the Vivado IP Integrator**
  Describes the different Versal ACAP design flows and covers the platform creation process using the Vivado IP integrator. {Lecture, Lab}

Day 2

Clocking and I/O Resources in the Versal ACAP Architecture

- **Versal ACAP: Clocking Architecture**
  Discusses the clocking architecture, clock buffers, clock routing, clock management functions, and clock de-skew in the Versal ACAP. {Lecture}
- **Versal ACAP: SelectIO Resources**
  Describes the I/O bank, SelectIO interface, and I/O delay features in the Versal ACAP. {Lecture, Lab}

Timing – Intermediate

- **Timing Constraints Editor**
  Introduces the timing constraints editor tool for creating timing constraints. {Lecture}
- **Report Clock Networks**
  Demonstrates how to use the `report_clock_networks` command to view the primary and generated clocks in a design. {Lecture, Demo}
- **Timing Summary Report**
  Reviews how to use the post-implementation timing summary report to sign off for timing closure. {Lecture, Demo}
- **Clock Group Constraints**
  Describes applying clock group constraints for asynchronous clock domains. {Lecture, Demo}
- **Introduction to Timing Exceptions**
  Introduces timing exception constraints and applying them to fine tune design timing. {Lecture, Demo, Lab}

Power

- **Power Analysis and Optimization Using the Vivado Design Suite**
  Illustrates using report power commands to estimate power consumption. {Lecture, Lab}

Configuration

- **Configuration Process**
  Reviews the FPGA configuration process, such as device power up and CRC checks. {Lecture}

Debugging

- **HDL Instantiation Debug Probing Flow**
  Covers the HDL instantiation flow to create and instantiate a VIO core and observe its behavior using the Vivado logic analyzer. {Lecture, Lab}

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Visit **morgan-aps.com/training**, for full course schedule and training information.

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

Morgan A.P.S. Course Cancellation Policy

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.

Online training with real hardware

During the Covid-19 period, some companies do not allow their staff to participate in live in-person training.

- Consequently, Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your Xilinx based device quickly and efficiently.