

Course Description

This course shows you how to build an effective FPGA design using synchronous design techniques, using the Vivado® IP integrator to create a sub-system, using proper HDL coding techniques to improve design performance, and debugging a design with multiple clock domains.

Level – FPGA 2

Course Duration – 2 days

Price – \$1,600 or 16 Xilinx Training Credits

Course Part Number – FPGA-VDES2-ILT

Who Should Attend? – Digital designers who have a working knowledge of HDL (VHDL or Verilog) and who are new to Xilinx FPGAs

Prerequisites

- [Designing FPGAs Using the Vivado Design Suite 1](#) course
- Working HDL knowledge (VHDL or Verilog)
- Digital design experience

Optional Videos

- Basic HDL Coding Techniques*

Software Tools

- Vivado Design or System Edition 2018.1

Hardware

- Architecture: UltraScale™ and 7 series FPGAs**
- Demo board (optional): Kintex®-7 FPGA KC705 board**

* This course focuses on the UltraScale and 7 series architectures.

** Check with [Morgan Advanced Programmable Systems, Inc.](#) for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Identify synchronous design techniques
- Build resets into your system for optimum reliability and design speed
- Create a Tcl script to create a project, add sources, and implement a design
- Describe and use the clock resources in a design
- Create and package your own IP and add to the Vivado IP catalog to reuse
- Use the Vivado IP integrator to create a block design
- Apply timing exception constraints in a design as part of the Baselining procedure to fine tune the design
- Describe how power analysis and optimization is performed
- Describe the HDL instantiation flow of the Vivado logic analyzer

Course Outline

Day 1

- UltraFast Design Methodology: Design Creation {Lecture}
- Synchronous Design Techniques {Lecture}
- Resets {Lecture, Lab}
- Register Duplication {Lecture}
- Scripting in Vivado Design Suite Project Mode {Lecture, Lab}
- Clocking Resources {Lectures, Lab}
- I/O Logic Resources {Lectures}
- Creating and Packaging Custom IP {Lecture, Lab}

Day 2

- Using an IP Container {Lecture, Demo}
- Designing with the IP Integrator {Lecture, Lab, Demo, Case Study}
- Timing Constraints Editor {Lecture}

- Report Clock Networks {Lecture, Demo}
- Timing Summary Report {Lecture, Demo}
- Clock Group Constraints {Lecture, Demo}
- Introduction to Timing Exceptions {Lecture, Lab, Demo}
- Power Analysis and Optimization Using the Vivado Design Suite {Lecture, Lab}
- Configuration Process {Lecture}
- HDL Instantiation Debug Probing Flow {Lecture, Lab}
- Design Analysis Using Tcl Commands {Lecture, Demo, Lab}

Topic Descriptions

Day 1

- UltraFast Design Methodology: Design Creation – Overview of the methodology guidelines covered in this course.
- Synchronous Design Techniques – Introduces synchronous design techniques used in an FPGA design.
- Resets – Investigates the impact of using asynchronous resets in a design.
- Register Duplication – Use register duplication to reduce high fanout nets in a design.
- Scripting in Vivado Design Suite Project Mode – Explains how to write Tcl commands in the project-based flow for a design.
- Clocking Resources – Describes various clock resources, clocking layout, and routing in a design.
- I/O Logic Resources – Overview of I/O resources and the IOB property for timing closure.
- Creating and Packaging Custom IP – Create your own IP and package and include it in the Vivado IP catalog.

Day 2

- Using an IP Container – Use a core container file as a single file representation for an IP.
- Designing with the IP Integrator – Use the Vivado IP integrator to create the uart_led subsystem.
- Timing Constraints Editor – Introduces the timing constraints editor tool to create timing constraints.
- Report Clock Networks – Use `report clock networks` to view the primary and generated clocks in a design.
- Timing Summary Report – Use the post-implementation timing summary report to sign-off criteria for timing closure.
- Clock Group Constraints – Apply clock group constraints for asynchronous clock domains.
- Introduction to Timing Exceptions – Introduces timing exception constraints and applying them to fine tune design timing.
- Power Analysis and Optimization Using the Vivado Design Suite – Use report power commands to estimate power consumption.
- Configuration Process – Understand the FPGA configuration process, such as device power up, CRC check, etc.
- HDL Instantiation Debug Probing Flow – Covers the HDL instantiation flow to create and instantiate a VIO core and observe its behavior using the Vivado logic analyzer.
- Design Analysis Using Tcl Commands – Analyze a design using Tcl commands.

Register Today

Morgan Advanced Programmable Systems, Inc. (MAPS, Inc.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota and Wisconsin.

Visit morgan-aps.com/training, for full course schedule and training information.



You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

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- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent [here](#).

MAPS Inc. Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- MAPS may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
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