Advanced Tools and Techniques of the Vivado Design Suite

FPGA 4

FPGA-VATT-ILT (v1.0)

Course Specification

Course Description

This course tackles the most sophisticated aspects of the Vivado® Design Suite and Xilinx hardware. Learn to utilize advanced static timing analysis and apply timing constraints for source-synchronous and system-synchronous interfaces. Utilize floorplanning techniques to improve design performance and use Tcl scripting in both the project-based and non-project batch design flows.

Level – FPGA 4

Course Duration – 2 days

Price – $1,600 or 16 Xilinx Training Credits

Course Part Number – FPGA-VATT-ILT

Who Should Attend? – Engineers who seek advanced training in using Xilinx tools to improve FPGA performance and utilization while also increasing productivity

Prerequisites

- *Essentials of FPGA Design* course
- *Vivado Design Suite Static Timing Analysis and Xilinx Design Constraints* course
- Intermediate knowledge of Verilog or VHDL is strongly recommended
- At least six months of design experience with Xilinx tools and FPGAs

Software Tools

- Vivado Design or System Edition 2015.3

Hardware

- Architecture: UltraScale™ and 7 series FPGAs*
- Demo board: None*

* This course focuses on the UltraScale and 7 series architectures.

** Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Explain the impact that manufacturing process variations have on timing analysis
- Describe how min/max timing analysis information is conveyed in a timing report
- Utilize the custom timing report options to build optimal timing reports
- Utilize some of the advanced timing report features to control how delay paths are displayed in timing reports
- Make appropriate I/O timing constraints and design modifications for source-synchronous and system-synchronous interfaces
- Analyze a timing report to identify how to center the clock in the data eye
- Utilize the most advanced features (area constraints) of the Vivado IDE to improve design performance
- Use the Hierarchical viewer, Schematic viewer, and timing report information to make the best area constraints
- Use scripting in project-based and non-project batch flows to synthesize, implement, and generate custom timing reports

Course Outline

Day 1

- Review of the *Vivado Design Suite Static Timing Analysis and Xilinx Design Constraints* course
- UltraFast Design Methodology
- Advanced Timing Analysis
- Demo: Timing Reports
- System-Synchronous and Source-Synchronous I/O Timing
- Demo: System-Synchronous I/O Timing
- **Lab 1:** Advanced I/O Timing
- Incremental Compile in Implementation
- Introduction to Pblocks

Day 2

- Floorplanning Techniques
- **Lab 2:** Design Analysis and Floorplanning
- Hierarchical Design
- Project-Based and Non-Project Batch Design Flows
- Scripting Using the Project-Based and Non-Project Batch Flows
- **Lab 3a:** Scripting in the Project-Based Flow
- **Lab 3b**: Scripting in the Non-Project Batch Flow
- Appendix: HDL Coding Techniques
- Appendix: Advanced Timing Analysis

Lab Descriptions

- **Lab 1:** Advanced I/O Timing – Make I/O timing constraints for a source-synchronous, double data rate (DDR) interface. Perform a static timing analysis of the interfaces to determine the optimal clock and data relationship for maximum setup and hold-time margin. Finally, adjust the data path delay to realize the optimal timing solution.
- **Lab 2:** Design Analysis and Floorplanning – Explore the pre- and post-implementation design analysis features of the Vivado IDE. These features enable early detection of potential design issues, exploration of alternate devices, and floorplanning.
- **Lab 3a:** Scripting in the Project-Based Flow – Write Tcl commands in the project-based flow for the design process (from creating a new project through implementation).
- **Lab 3b**: Scripting in the Non-Project Batch Flow – Write Tcl commands in the non-project batch flow for the design process (from creating a new project through implementation).

Register Today

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Visit **morgan-aps.com/training**, for full course schedule and training information.

Morgan Advanced Programmable Systems

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

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- Student cancellations must be sent here.

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