Vivado Design Suite for ISE Software Project Navigator Users

FPGA 2

FPGA-V4ISE-ILT (v1.0)

Course Specification

Course Description

This course offers introductory training on the Vivado® Design Suite. This course is for experienced ISE® software users who want to take full advantage of the Vivado Design Suite feature set. Learn about the Vivado Design Suite projects, design flow, Xilinx Design Constraints, and basic timing reports.

Level – FPGA 2

Course Duration – 2 days

Price – $1,600 or 16 Xilinx Training Credits

Course Part Number – FPGA-V4ISE-ILT

Who Should Attend? – Existing Xilinx ISE software Project Navigator FPGA designers

Prerequisites

- Basic knowledge of the VHDL or Verilog language
- Digital design knowledge

Recommended Recorded Videos

- Basic FPGA Architecture: Slice and I/O Resources
- Basic FPGA Architecture: Memory and Clocking Resources

Software Tools

- Vivado Design or System Edition 2018.1

Hardware

- Architecture: UltraScale™ and 7 series FPGAs*
- Demo board (optional): Kintex® UltraScale FPGA KCU105 board or Kintex-7 FPGA KC705 board*

* This course focuses on the UltraScale and 7 series architectures.

** Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Use the Project Manager in the Vivado Design Suite to start a new project
- Identify the available Vivado IDE design flows (project based and non-project batch)
- Identify file sets (HDL, XDC, simulation) and analyze designs using the cross-selection capabilities, Schematic viewer, and Hierarchical viewer
- Synthesize and implement an HDL design
- Apply HDL coding techniques and reset methodology to your design
- Utilize a systematic approach to apply synchronous design techniques
- Use the Vivado IP flow to add and customize IPs
- Explain how to use Tcl commands and scripts in your design
- Write Tcl scripts in Vivado Design Suite project and non-project modes

Course Outline

Day 1

- Introduction to the Vivado Design Suite {Lecture}
- Introduction to Vivado Design Flows {Lecture}
- Vivado Design Suite Project Mode {Lecture, Lab}
- Behavioral Simulation {Lecture}
- Synthesis and Implementation {Lecture, Lab}
- Basic Design Analysis in the Vivado IDE {Lab, Demo}
- Vivado Design Suite I/O Pin Planning {Lecture, Lab}
- Xilinx Power Estimator Spreadsheet {Lecture}
- UltraFast Design Methodology: Board and Device Planning {Lecture, Demo}
- HDL Coding Techniques {Lecture}
- Resets {Lecture, Lab}
- Register Duplication {Lecture}
- Synchronous Design Techniques {Lecture}

Day 2

- Vivado IP Flow {Lecture, Lab, Demo}
- Designing with the IP Integrator {Lecture, Lab, Demo, Case Study}
- UltraFast Design Methodology: Design Creation {Lecture}
- Vivado Design Suite Non-Project Mode {Lecture}
- Introduction to the Tcl Environment {Lecture, Lab}
- Design Analysis Using Tcl Commands {Lecture, Lab, Demo}
- Scripting in Vivado Design Suite Project Mode {Lecture, Lab}
- Scripting in Vivado Design Suite Non-Project Mode {Lecture, Lab}

Topic Descriptions

Day 1

- Introduction to the Vivado Design Suite – Introduces the Vivado Design Suite.
- Introduction to Vivado Design Flows – Introduces the Vivado design flows: the project flow and non-project batch flow.
- Vivado Design Suite Project Mode – Create a project, add files to the project, explore the Vivado IDE, and simulate the design.
- Behavioral Simulation – Performs behavioral simulation for your design.
- Synthesis and Implementation – Create timing constraints according to the design scenario and synthesize and implement the design.
- Basic Design Analysis in the Vivado IDE – Use the various design analysis features in the Vivado Design Suite.
- Vivado Design Suite I/O Pin Planning – Use the I/O Pin Planning layout to perform pin assignments in a design.
- Xilinx Power Estimator Spreadsheet – Estimate the amount of resources and default activity rates for a design and evaluate the estimated power calculated by XPE.
- UltraFast Design Methodology: Board and Device Planning – Introduces the methodology guidelines covered in this course and the UltraFast Design Methodology checklist.
- HDL Coding Techniques – Covers basic digital coding guidelines used in an FPGA design.
- Resets – Investigates the impact of using asynchronous resets in a design.
- Register Duplication – Use register duplication to reduce high fanout nets in a design.
- Synchronous Design Techniques – Introduces synchronous design techniques used in an FPGA design.

Day 2

- Vivado IP Flow – Customize IP, instantiate IP, and verify the hierarchy of your design IP.
- Designing with the IP Integrator – Use the Vivado IP integrator to create the uart_led subsystem.
- UltraFast Design Methodology: Design Creation – Overview of the methodology guidelines covered in this course.
- Vivado Design Suite Non-Project Mode – Create a design in the Vivado Design Suite non-project mode.
- Introduction to the Tcl Environment – Introduces Tcl (tool command language).

- Design Analysis Using Tcl Commands – Analyze a design using Tcl commands.
- Scripting in Vivado Design Suite Project Mode – Explains how to write Tcl commands in the project-based flow for a design.
- Scripting in Vivado Design Suite Non-Project Mode – Write Tcl commands in the non-project batch flow for a design.

Register Today

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

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