UltraScale Architecture Design Migration Workshop

FPGA 3

FPGA-USM-ILT (v1.0)

Course Specification

Course Description

This course introduces new and experienced designers to an efficient methodology for FPGA design migration to the UltraScale™ architecture. This course is targeted towards designers who have used the Vivado® Design Suite and are already familiar with UltraScale architecture features.

In this course you will learn how to best migrate your design and IP to the UltraScale architecture and the best way to use the Vivado Design Suite during design migration. The lab allows for practical hands-on experience of the principles taught.

Level – FPGA 3

Course Duration – 1/2 day

Price – $500 or 5 Xilinx Training Credits

Course Part Number – FPGA-USM-ILT

Who Should Attend? – Anyone who would like to build a design for the UltraScale device family and has been introduced to the UltraScale device features.

Prerequisites

- *Designing FPGAs Using the Vivado Design Suite 1* course
- Intermediate VHDL or Verilog knowledge

Software Tools

- Vivado HL Design or System Edition 2018.1

Hardware

- Architecture: UltraScale FPGAs*
- Demo board: None*

* This course focuses on design migration to the UltraScale architecture.

** Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Recognize the limitations of the Vivado Design Suite and its ability to synthesize for the new UltraScale architecture resources
- Describe the recommended IP migration methodology
- Use beneficial Vivado Design Suite utilities and reports to migrate the designs to UltraScale FPGAs

Course Outline

- FPGA Design Migration {Lecture, Lab}
- Design Migration Methodology {Lecture}
- 10G PCS/PMA and MAC Design Migration {Lab}

Topic Descriptions

- FPGA Design Migration – Migrate an existing 7 series design to the UltraScale architecture.
- Design Migration Methodology – Review the migration methodology recommended by Xilinx for design migrations.
- 10G PCS/PMA and MAC Design Migration – Migrate a successfully implemented 7 series design containing the 10G Ethernet MAC and 10G PCS/PMA IP to an UltraScale FPGA.

Register Today

Morgan Advanced Programmable Systems, Inc. (MAPS, Inc.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota and Wisconsin.

Visit **morgan-aps.com/training**, for full course schedule and training information.

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

MAPS Inc. Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- MAPS may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
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- For additional information or to schedule a private class contact us here.

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