UltraScale and UltraScale+ Architectures Workshop

FPGA 3

FPGA-US1D (v1.0)

Course Specification

Course Description

This is a one-day version of the *Designing with the UltraScale and UltraScale+ Architectures* course and introduces new and experienced designers to the most sophisticated aspects of the UltraScale™ and UltraScale+™ architectures. Targeted towards designers who have used the Vivado® Design Suite, this course focuses on designing for the new and enhanced resources found in our newest FPGA family.

Topics covered include an introduction to the clock management resources (MMCM and PLL), global and regional clocking resources, memory resources, and source-synchronous resources. A description of the improvements to the dedicated transceivers and Transceiver Wizard is also included. Use of the Memory Interface Generator (MIG) and the new DDR4 memory interface capabilities is also covered.

In addition, you will learn how to best migrate your design and IP to the UltraScale architecture and the best way to use the Vivado Design Suite during design migration. A combination of modules and labs allow for practical hands-on experience of the principles taught.

Level – FPGA 3

Course Details

- 1 day live instructor led training (online or in person)
- 14 lectures
- 8 labs
- 1 demo

Price – $800 or 8 Xilinx Training Credits

Course Part Number – FPGA-US1D

Who Should Attend? – Anyone who would like to build a design for the UltraScale or UltraScale+ device family

Prerequisites

- Designing FPGAs Using the Vivado Design Suite 1
- Intermediate VHDL or Verilog knowledge

Software Tools

- Vivado HL Design or System Edition 2020.1

Hardware

- Architecture: UltraScale and UltraScale+ FPGAs*
- Demo board: None*

* This course focuses on the UltraScale and UltraScale+ architectures. Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Take advantage of the primary UltraScale architecture resources
- Define the block RAM and FIFO resources available for UltraScale FPGAs
- Describe the UltraRAM features
- Properly design for the I/O and SERDES resources
- Identify the MMCM, PLL, and clock routing resources included with the UltraScale architecture
- Identify the hard IP resources available for implementing high-performance DDR4 physical layer interfaces
- Describe the additional features of the dedicated transceivers
- Effectively migrate your IP and design to the UltraScale architecture as quickly as possible

Course Outline

- **UltraScale Architecture CLB Resources**
  Examine the CLB resources, such as the LUT and the dedicated carry chain, in the UltraScale architecture. {Lecture, Lab}
- **UltraScale Architecture Clocking Resources**
  Use the Clocking Wizard to configure a clocking subsystem to provide various clock outputs and distribute them on the dedicated global clock networks. {Lectures, Lab}
- **FPGA Design Migration**
  Migrate an existing 7 series design to the UltraScale architecture. {Lecture, Lab}
- **UltraScale Architecture Block Memory Resources**
  Review the block RAM resources in the UltraScale architecture. {Lecture}
- **UltraScale Architecture FIFO Memory Resources**
  Review the FIFO resources in the UltraScale architecture. {Lecture}
- **UltraRAM Memory**
  Use UltraRAM for a design requiring a larger memory size than block RAM. {Lecture, Lab}
- **DDR4 Design Creation Using MIG**
  Create a DDR4 memory controller with the Memory Interface Generator (MIG) utility. {Lab}
- **UltraScale Architecture I/O Resources Overview**
  Provides an overview of the I/O resources in the UltraScale architecture. {Lecture}
- **UltraScale Architecture I/O Resources: Component Mode**
  Implement a high-performance, source-synchronous interface using I/O resources in Component mode for the UltraScale architecture. {Lecture, Lab}
- **UltraScale Architecture I/O Resources: Native Mode**
  Implement a high-performance, source-synchronous interface using I/O resources in Native mode for the UltraScale architecture. {Lecture, Lab}
- **UltraScale Architecture Transceivers**
  Review the enhanced features of the transceivers in the UltraScale architecture. {Lecture}
- **UltraScale FPGAs Transceivers Wizard**
  Use the Transceivers Wizard to build a design that uses a single serial transceiver and observe the created file structures. {Lecture, Lab}

Register Today

Morgan Advanced Programmable Systems, Inc. (Morgan A.P.S.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota and Wisconsin.

Visit morgan-aps.com/training, for full course schedule and training information.

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

Morgan A.P.S. Course Cancellation Policy

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.

Online training with real hardware

During the Covid-19 period, some companies do not allow their staff to participate in live in- person training.

- Consequently, Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are setup in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your Xilinx based device quickly and efficiently.