Designing with the UltraScale and UltraScale+ Architectures

FPGA-US (v1.0)

Course Specification

Course Description

This course introduces the UltraScale™ and UltraScale+™ architectures to both new and experienced designers.

The emphasis is on:

- Introducing CLB resources, clock management resources (MMCM and PLL), global and regional clocking resources, memory and DSP resources, and source-synchronous resources
- Describing improvements to the dedicated transceivers and Transceiver Wizard
- Reviewing the Memory Interface Generator (MIG) and DDR4 memory interface capabilities
- Migrating existing designs and IP to the UltraScale architecture with optimal use of the Vivado® Design Suite

What's New for 2022.2

- Added content to the HDL Coding Techniques module
- All labs have been updated to the latest software versions

Level – FPGA 3

Course Details

- 2 days live instructor led training (online or in-person)
- 21 lectures
- 13 labs
- 2 demos

Price –$1,600 or 16 Xilinx Training Credits

Course Part Number – FPGA-US

Who Should Attend? – Anyone who would like to build a design for the UltraScale or UltraScale+ device family

Prerequisites

- Designing FPGAs Using the Vivado Design Suite 1
- Intermediate VHDL or Verilog knowledge

Companion Course

- Vivado Static Timing Analysis, Xilinx Design Constraints, and Advanced Techniques of the Vivado Design Suite

Software Tools

- Vivado Design Suite 2022.2

Hardware

- Architecture: UltraScale and UltraScale+ FPGAs*
- Demo board: None*

* This course focuses on the UltraScale and UltraScale+ architectures. Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

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After completing this comprehensive training, you will have the necessary skills to:

- Take advantage of the primary UltraScale architecture resources
- Describe the new CLB capabilities and the impact that they make on your HDL coding style
- Define the block RAM, FIFO, and DSP resources available
- Describe the new type of memory structures available in UltraScale+™ devices, such as UltraRAM and the high bandwidth memory (HBM) available in Virtex® UltraScale+ devices
- Properly design for the I/O and SERDES resources
- Identify the MMCM, PLL, and clock routing resources included
- Identify the hard IP resources available for implementing high-performance DDR4 memory interfaces
- Describe the additional features of the dedicated transceivers
- Effectively migrate your IP and design to the UltraScale architecture as quickly as possible

Course Outline

Day 1

- **Introduction to the UltraScale Architecture**
  Review the UltraScale architecture, which includes enhanced CLB resources, DSP resources, etc. {Lecture}
- **UltraScale Architecture CLB Resources**
  Examine the CLB resources, such as the LUT and the dedicated carry chain, in the UltraScale architecture. {Lecture, Lab}
- **HDL Coding Techniques**
  Covers basic digital coding guidelines used in an FPGA design. {Lecture, Lab}
- **UltraScale Architecture Clocking Resources**
  Use the Clocking Wizard to configure a clocking subsystem to provide various clock outputs and distribute them on the dedicated global clock networks. {Lectures, Lab}
- **FPGA Design Migration**
  Migrate an existing 7 series design to the UltraScale architecture. {Lecture, Lab}
- **Clocking Migration**
  Migrate a 7 series design to the UltraScale architecture with a focus on clocking resources. {Lab}
- **UltraScale Architecture Block RAM Memory Resources**
  Review the block RAM resources in the UltraScale architecture. {Lecture}
- **UltraScale Architecture FIFO Memory Resources**
  Review the FIFO resources in the UltraScale architecture. {Lecture}
- **UltraRAM Memory**
  Use UltraRAM for a design requiring a larger memory size than block RAM. {Lecture, Lab}
- **High Bandwidth Memory**
  Use high bandwidth memory (HBM) for applications requiring high bandwidth. {Lecture, Demo}

Day 2

- **UltraScale Architecture DSP Resources**
  Review the DSP resources in the UltraScale architecture. {Lecture, Lab}
- **Design Migration Software Recommendations**
  List the Xilinx software recommendations for design migrations from 7 series to the UltraScale architecture. {Lecture}
- **DDR3 MIG Design Migration**
  Migrate a 7 series MIG design to the UltraScale architecture. {Lab}
- **DDR4 Design Creation Using MIG**
  Create a DDR4 memory controller with the Memory Interface Generator (MIG) utility. {Lab}
- **UltraScale Architecture I/O Resources Overview**
  Review the I/O resources in the UltraScale architecture. {Lecture}
- **UltraScale Architecture I/O Resources: Component Mode**

Implement a high-performance, source-synchronous interface using I/O resources in Component mode for the UltraScale architecture. {Lecture, Lab}

- **UltraScale Architecture I/O Resources: Native Mode**
  Implement a high-performance, source-synchronous interface using I/O resources in Native mode for the UltraScale architecture. {Lecture, Lab}
- **Design Migration Methodology**
  Review the migration methodology recommended by Xilinx for design migrations. {Lecture}
- **10G PCS/PMA and MAC Design Migration**
  Migrate a successfully implemented 7 series design containing the 10G Ethernet MAC and 10G PCS/PMA IP to an UltraScale FPGA. {Lab}
- **UltraScale Architecture Transceivers**
  Review the enhanced features of the transceivers in the UltraScale architecture. {Lecture}
- **UltraScale FPGAs Transceivers Wizard**
  Use the Transceivers Wizard to build a design that uses a single serial transceiver and observe the created file structures. {Lecture, Demo, Lab}
- **Introduction to the UltraScale+ Families**
  Identify the enhancements made to the UltraScale architecture in the UltraScale+ architecture families. {Lecture}

Register Today

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Visit **morgan-aps.com/training**, for full course schedule and training information.

Morgan Advanced Programmable Systems

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

Morgan A.P.S. Course Cancellation Policy

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.

Online training with real hardware

During the Covid-19 period, some companies do not allow their staff to participate in live in-person training.

- Consequently, Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your Xilinx based device quickly and efficiently.