Designing with the IP Integrator Tool

FPGA-IPI (v1.0)

Course Specification

Course Description

Explore the Vivado™ IP integrator tool and its features to gain the expertise needed to develop, implement, and debug different IP integrator block designs using the Vivado Design Suite.

This course focuses on:

- Creating an IP integrator block design using the Vivado Design Suite
- Creating your own custom IP via the IP packaging flow
- Using the block design container (BDC) and module referencing features of the IP integrator
- Using the IP integrator to add and configure the Versal™ device CIPS block and then to export the generated programmable device image (PDI)
- Configuring the AXI network on chip (NoC) to access DDR memory controllers in Versal devices

What's New for 2023.2

- Versal Adaptive SoC Tool Flow lab: Introduced the new Vitis™ Unified IDE
- All labs have been updated to the latest software versions

Level – FPGA 1

Course Details

- 2 days ILT or 16 hours On-Demand
  - 10 lectures
  - 10 labs
  - 2 demos

Price – $1,600 or 16 Xilinx Training Credits

Course Part Number – FPGA-IPI

Who Should Attend? – Software and hardware developers, system architects, and anyone who wants to learn about the Vivado Design Suite IP integrator tool

Prerequisites

- Basic knowledge of AMD FPGAs and adaptive SoCs

Alternative Courses

- EMBD-88080: Xilinx Rapid Development Embedded Design
- EMBD-ZUPSA: Zynq UltraScale+ MPSoC for the System Architect

Software Tools

- Vivado Design Suite 2023.2
- Vitis Unified IDE 2023.2

Hardware

- Architecture: UltraScale™ family and Versal adaptive SoCs
- Demo board: Zynq™ UltraScale+™ ZCU104 board

Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the Vivado tool flow for RTL-based and IP-based design flows
- Create a Vivado IP integrator block design using the Vivado Design Suite
- Describe the block design container feature in the IP integrator
- Package custom IP and add it to the IP catalog repository or manage it from a remote location
- Add an RTL module or a block design (BD) into a block design by using RTL module referencing
- Add and configure the Versal device CIPS block and export the generated hardware
- Configure the AXI NoC to access DDR memory controllers in Versal devices
- Debug a design by adding debug cores using the IP integrator
- Use a revision control system in the Vivado Design Suite flows

Course Outline

Day 1

Vivado IP Catalog

- **Vivado IP Flow**
  Demonstrates how to customize IP, instantiate IP, and verify the hierarchy of your design IP. {Lecture, Demo}

Using the Vivado IP Integrator

- **Getting Started with Vivado IP Integrator**
  Introduces the Vivado IP integrator tool and its features. Also reviews creating and working with block designs. {Lecture, Demo, Lab}
- **Designing IP Subsystems Using Vivado IP Integrator**
  Illustrates designing with processor-based subsystems and working with custom RTL code. Also explains how to create Vitis platforms using Vivado IP integrator. {Lecture, Lab}
- **Block Design Containers in the Vivado IP Integrator**
  Describes the block design container (BDC) feature and shows how to create a BDC in the IP integrator. {Lecture, Lab}
- **Creating and Packaging Custom IP**
  Covers creating your own IP and package and including it in the Vivado IP catalog. {Lecture, Lab}
- **Module Referencing in IP Integrator**
  Shows how to quickly add an RTL module or a block design (BD) into a block design by using RTL module referencing. {Lab}

Day 2

- **Versal Adaptive SoC: Hardware Platform Development Using the Vivado IP Integrator**
  Describes the different Versal device design flows and covers the platform creation process using the Vivado IP integrator. {Lecture, Lab}
- **Versal Adaptive SoC: NoC Introduction and Concepts**
  Reviews the basic vocabulary and high-level operations of the NoC. {Lecture, Labs}

Debugging

- **Debug Flow in an IP Integrator Block Design**
  Shows how to insert the debug cores into IP integrator block designs. {Lecture, Lab}

Version Control Systems

- **Revision Control Systems in the Vivado Design Suite**
  Investigates using version control systems with the Vivado design flows. {Lecture, Lab}

Vivado IP Catalog

- **Managing IP in Remote Locations**
  Covers storing IP and related files that are remote to the current working project directory. {Lecture}

Register Today

Morgan Advanced Programmable Systems, Inc. (Morgan A.P.S.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota, and Wisconsin.

Visit **morgan-aps.com/training**, for full course schedule and training information.

Morgan Advanced Programmable Systems

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

Morgan A.P.S. Course Cancellation Policy

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.

Online training with real hardware

During the Covid-19 period, some companies do not allow their staff to participate in live in-person training.

- Consequently, Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your Xilinx based device quickly and efficiently.