AMD XILINX

Designing with Dynamic Function eXchange (DFX) Using the Vivado Design Suite

FPGA-DFX (v1.0)

Course Specification

Course Description

Learn how to construct, implement, and download a Dynamic Function eXchange (DFX) FPGA design using the Vivado™ Design Suite. This course covers both the tool flow and mechanics of successfully creating a DFX design.

The emphasis of this course is on:

- Identifying best design practices and understanding the subtleties of the DFX design flow
- Using the DFX Controller and DFX Decoupler IP in the DFX process
- Implementing DFX in an embedded system environment
- Applying appropriate debugging techniques on DFX designs
- Employing best practice coding styles for a DFX system

What's New for 2022.2

- Added Versal™ adaptive SoC support for the Abstract Shell feature
- Added lab on Abstract Shell project mode
- Updated the DFX design considerations for Versal devices
- Added information on reconfiguring using partial PDI files for Versal devices
- Added recommendations for floorplanning constraints
- All labs have been updated to the latest software versions

Level – FPGA 4

Course Details

- 2 days ILT
- 19 lectures
- 10 labs
- 2 demos (ILT only)

Price – $1,600.00 or 16 Xilinx Training Credits

Course Part Number – FPGA-DFX

Who Should Attend? – Digital designers who have a working knowledge of HDL (VHDL or Verilog) and digital design and who want to implement Dynamic Function eXchange techniques

Prerequisites

- Designing FPGAs Using the Vivado Design Suite 1
- Designing FPGAs Using the Vivado Design Suite 2
- Designing FPGAs Using the Vivado Design Suite 3
- Designing FPGAs Using the Vivado Design Suite 4
- Working HDL knowledge (VHDL or Verilog)

Software Tools

- Vivado Design Suite 2022.2
- Vitis™ Unified Software Platform 2022.2

Hardware

- Architecture: UltraScale™ FPGAs and Versal adaptive SoCs*
- Demo board:
  - Zynq™ UltraScale+™ MPSoC ZCU104 board*
  - Versal adaptive SoC VCK190 board*

* Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe what Dynamic Function eXchange is
- Define DFX regions and reconfigurable modules with the Vivado Design Suite
- Generate the appropriate full and partial bitstreams for a DFX design
- Implement a nested DFX design
- Enable the Abstract Shell feature in project mode
- Use the ICAP and PCAP components to deliver partially reconfigurable systems
- Implement a DFX system using the DFX Controller IP
- Use the block design container feature of the Vivado IP integrator to create a DFX design
- Identify how Dynamic Function eXchange affects various silicon resources, including block RAM, IOBs, fabric, and MGTs
- Implement a Dynamic Function eXchange system using the following techniques:
  - Direct JTAG connection, floorplanning, and timing constraints and analysis
- Debug a DFX design using the Vivado Design Suite
- Implement a DFX system in an embedded environment using the Vitis IDE

Course Outline

Day 1

Basics of DFX

- **Introduction to Dynamic Function eXchange (DFX)**
  Explains what Dynamic Function eXchange is and defines the terminologies used in DFX. Also provides an overview of the configuration and reconfiguration processes. {Lecture, Demo}

DFX Tool Flow

- **DFX Flow Using the Vivado Design Suite GUI**
  Illustrates the steps for creating a DFX project in the Vivado Design Suite and describes various supported and unsupported features. {Lecture, Lab}
- **DFX Flow Using Vivado Design Suite Tcl Commands**
  Reviews the flow using non-project-based commands, including using implementation constraints and specific characteristics. {Lecture, Lab}
- **Nested DFX**
  Describes using nested DFX, the process by which a Reconfigurable Partition (RP) can be segmented into smaller regions, each of which is partially reconfigurable. {Lecture, Lab}
- **Abstract Shell for Dynamic Function eXchange**
  Describes how compilation time can be reduced by using an Abstract Shell. {Lecture, Lab}

DFX Design Considerations for AMD Devices

- **DFX Design Considerations for All AMD Devices**
  Covers the requirements, characteristics, and limitations associated with DFX designs that can simplify the debug process and reduce the risk of design malfunctions. {Lecture}
- **DFX Design Considerations for 7 Series, Zynq SoC, UltraScale, and UltraScale+ Devices**
  Discusses DFX design consideration methodologies for various Xilinx device families. {Lecture}
- **DFX Design Considerations for Versal Devices**
  Describes the DFX design requirements that are specific to Versal devices. {Lecture}

DFX Design-Specific IP Blocks

- **DFX Intellectual Property (IP)**
  Reviews the various IPs that are specifically for use with DFX designs. {Lecture, Lab, Demo}
- **DFX Block Design Containers in IP Integrator**
  Describes the block design container feature and how BDCs enable DFX. {Lecture, Lab}

Day 2

DFX Configuration

- **Configuring Devices Using DFX**
  Reviews the basics of configuration and various configuration modes. {Lecture}
- **Configuration Parameters**
  Covers various configuration parameters, including factors that affect configuration time and configuration debugging. {Lecture}
- **DFX Bitstreams**
  Describes the different types of bitstreams for DFX compilation, including full, partial, blanking, and clearing. {Lecture}
- **DFX Bitstream Integrity**
  Describes partial bit file integrity and implementing DFX through the ICAP for FPGA devices. {Lecture}

DFX Design Analysis and Debugging

- **Floorplanning a DFX Design**
  Demonstrates how to create Pblocks for various devices and how to create a floorplan for a reconfigurable region. {Lecture, Lab}
- **DFX Timing Analysis and Constraints**
  Illustrates how and when to apply different constraint files, the process of performing a DFX timing-level simulation, and the process of performing static timing analysis on a DFX design. {Lecture, Lab}
- **DFX Debugging**
  Illustrates DFX debugging techniques using Vivado Design Suite debug cores. {Lecture, Lab}

DFX Designs in Embedded Systems

- **DFX in Embedded Systems**
  Describes the embedded design flow in the Vivado Design Suite, the advantages of using a processor with DFX, and how to connect a processor to the PCAP to control DFX using the Vitis IDE. {Lecture, Lab}
- **DFX Designs Using the PCIe Core**
  Reviews the advantages of using a PCIe core in a DFX design. {Lecture}

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Morgan Advanced Programmable Systems, Inc. (Morgan A.P.S.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota, and Wisconsin.

Visit **morgan-aps.com/training**, for full course schedule and training information.

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- You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

Morgan A.P.S. Course Cancellation Policy

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.

Online training with real hardware

- During the Covid-19 period, some companies do not allow their staff to participate in live in-person training.
- Consequently, Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your Xilinx based device quickly and efficiently.