Designing with the 7 Series Families

FPGA 3

FPGA-7SERIES (v1.0)

Course Specification

Course Description

Learn how to effectively utilize and properly design for the primary architectural resources found in 7 series devices.

The focus is on:

- Utilizing 7 series CLB, clocking, memory, DSP, and I/O resources
- Describing the dedicated hardware resources available (PCI Express® technology, analog-to-digital converters, and gigabit transceivers)
- Employing proper HDL coding techniques to get the most out of device resources

This course supports both experienced and less experienced FPGA designers who have already completed the *Designing FPGAs Using the Vivado Design Suite 1* course.

Level – FPGA 3

Course Duration – 2 days live instructor led training (in person or online)

Price – $1,600 or 16 Xilinx Training Credits

Course Part Number – FPGA-7SERIES

Who Should Attend? – Students who have previously taken the *Designing FPGAs Using the Vivado Design Suite 1* course

Prerequisites

- *Designing FPGAs Using the Vivado Design Suite 1* course
- Intermediate VHDL or Verilog knowledge

Software Tool

- Vivado® HL Design or System Edition 2017.3

Hardware

- Architecture: Artix®-7, Spartan®-7, Kintex®-7, and Virtex®-7 FPGAs
- Demo board: None

* This course focuses on the 7 series FPGA architectures.

** Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe all the functionality of the 6-input LUT and the CLB construction of the 7 series FPGAs
- Specify the CLB resources and the available slice configurations for the 7 series FPGAs
- Define the block RAM, FIFO, and DSP resources available for the 7 series FPGAs
- Properly design for the I/O block and SERDES resources
- Identify the MMCM, PLL, and clock routing resources included with these families
- Identify the hard resources available for implementing high performance DDR3 physical layer interfaces
- Describe the additional dedicated hardware for all the 7 series family members
- Properly code your HDL to get the most out of the 7 series FPGAs

Course Outline

Day 1

- Introduction to the 7 Series Architecture {Lecture}
- CLB Resources {Lecture, Lab}
- Slice Flip-Flops {Lecture}
- HDL Coding Techniques {Lecture, Lab}
- Clock Structure and Layout {Lecture}
- Clock Buffers {Lecture}
- Clock Management {Lecture}
- Clock Routing {Lecture}
- Using Clock Resources {Lecture, Lab}
- Dedicated Hardware Resources {Lecture}

Day 2

- Block RAM Memory Resources {Lecture, Lab}
- FIFO Memory Resources {Lecture}
- Memory Controllers {Lecture}
- DSP Resources {Lecture, Lab}
- I/O Resources Overview {Lecture}
- I/O Electrical Resources {Lecture}
- I/O Logical Resources {Lecture, Lab}
- Transceivers {Lecture}

Topic Descriptions

Day 1

- Introduction to the 7 Series Architecture – Review the 7 series architecture, which includes enhanced CLB resources, DSP resources, etc.
- CLB Resources – Examine the CLB resources, such as the LUT and the dedicated carry chain.
- Slice Flip-Flops – Examine the control sets and reset and initialization capabilities of the flip-flops.
- HDL Coding Techniques – Analyze a design that has asynchronous resets by generating various reports, such as the Timing Summary report and Utilization report. Convert the asynchronous resets to synchronous resets by removing the reset signal from the sensitivity list.
- Clocking Resources – Use the Clocking Wizard to configure a clocking subsystem to provide various clock outputs and distribute them on the dedicated global clock networks.
- Dedicated Hardware Resources – Examine the dedicated hardware IP in the 7 series architecture.

Day 2

- Block RAM Memory Resources – Review the block RAM resources.
- FIFO Memory Resources – Review the FIFO resources.
- Memory Controllers – Review the resources available in the 7 series architecture for implementing high-performance memory controllers.
- DSP Resources – Review the DSP resources.
- I/O Resources Overview – Overview of the I/O resources.
- I/O Electrical Resources – Review the I/O electrical resources.
- I/O Logical Resources – Review the I/O logical resources.
- Transceivers – Review the features of the transceivers.

Register Today

Morgan Advanced Programmable Systems, Inc. (Morgan A.P.S.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota and Wisconsin.

Visit morgan-aps.com/training, for full course schedule and training information.

Morgan Advanced Programmable Systems

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

Morgan A.P.S. Course Cancellation Policy

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.

Online training with real hardware

During the Covid-19 period, some companies do not allow their staff to participate in live in- person training.

- Consequently, Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are setup in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your Xilinx based device quickly and efficiently.