Designing with the 7 Series Families

FPGA 3

FPGA-7SERIES-ILT (v1.0)

Course Specification

Course Description

Are you interested in learning how to effectively utilize 7 series architectural resources? This course supports both experienced and less experienced FPGA designers who have already completed the *Designing FPGAs Using the Vivado Design Suite 1* course. This course focuses on understanding as well as how to properly design for the primary resources found in this popular device family.

Topics covered include device overviews, CLB construction, MMCM and PLL clocking resources, global, regional and I/O clocking techniques, memory, FIFO resources, DSP, and source-synchronous resources. Memory controller support and the dedicated hardware resources available in each of the families (PCI Express® technology, analog to digital converters and gigabit transceivers) are also introduced.

This course also includes a detailed discussion about proper HDL coding techniques that enables designers to avoid common mistakes and get the most out of their FPGA. A combination of modules and labs allow for practical hands-on application of the principles taught.

Level – FPGA 3

Course Duration – 2 days

Price – $1,600 or 16 Xilinx Training Credits

Course Part Number – FPGA-7SERIES-ILT

Who Should Attend? – Students who have previously taken the *Designing FPGAs Using the Vivado Design Suite 1* course

Prerequisites

- *Designing FPGAs Using the Vivado Design Suite 1* course
- Intermediate VHDL or Verilog knowledge

Software Tool

- Vivado® HL Design or System Edition 2017.3

Hardware

- Architecture: Artix®-7, Spartan®-7, Kintex®-7, and Virtex®-7 FPGAs
- Demo board: None

* This course focuses on the 7 series FPGA architectures.

** Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe all the functionality of the 6-input LUT and the CLB construction of the 7 series FPGAs
- Specify the CLB resources and the available slice configurations for the 7 series FPGAs
- Define the block RAM, FIFO, and DSP resources available for the 7 series FPGAs
- Properly design for the I/O block and SERDES resources
- Identify the MMCM, PLL, and clock routing resources included with these families
- Identify the hard resources available for implementing high performance DDR3 physical layer interfaces
- Describe the additional dedicated hardware for all the 7 series family members
- Properly code your HDL to get the most out of the 7 series FPGAs

Course Outline

Day 1

- Introduction to the 7 Series Architecture {Lecture}
- CLB Resources {Lecture, Lab}
- Slice Flip-Flops {Lecture}
- HDL Coding Techniques {Lecture, Lab}
- Clock Structure and Layout {Lecture}
- Clock Buffers {Lecture}
- Clock Management {Lecture}
- Clock Routing {Lecture}
- Using Clock Resources {Lecture, Lab}
- Dedicated Hardware Resources {Lecture}

Day 2

- Block RAM Memory Resources {Lecture, Lab}
- FIFO Memory Resources {Lecture}
- Memory Controllers {Lecture}
- DSP Resources {Lecture, Lab}
- I/O Resources Overview {Lecture}
- I/O Electrical Resources {Lecture}
- I/O Logical Resources {Lecture, Lab}
- Transceivers {Lecture}

Topic Descriptions

Day 1

- Introduction to the 7 Series Architecture – Review the 7 series architecture, which includes enhanced CLB resources, DSP resources, etc.
- CLB Resources – Examine the CLB resources, such as the LUT and the dedicated carry chain.
- Slice Flip-Flops – Examine the control sets and reset and initialization capabilities of the flip-flops.
- HDL Coding Techniques – Analyze a design that has asynchronous resets by generating various reports, such as the Timing Summary report and Utilization report. Convert the asynchronous resets to synchronous resets by removing the reset signal from the sensitivity list.
- Clocking Resources – Use the Clocking Wizard to configure a clocking subsystem to provide various clock outputs and distribute them on the dedicated global clock networks.
- Dedicated Hardware Resources – Examine the dedicated hardware IP in the 7 series architecture.

Day 2

- Block RAM Memory Resources – Review the block RAM resources.
- FIFO Memory Resources – Review the FIFO resources.
- Memory Controllers – Review the resources available in the 7 series architecture for implementing high-performance memory controllers.
- DSP Resources – Review the DSP resources.
- I/O Resources Overview – Overview of the I/O resources.
- I/O Electrical Resources – Review the I/O electrical resources.
- I/O Logical Resources – Review the I/O logical resources.
- Transceivers – Review the features of the transceivers.

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Morgan Advanced Programmable Systems

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

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- Student cancellations must be sent here.

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