Advanced FPGA Implementation

FPGA 4

FPGA33000-ILT (v1.0)

Course Specification

Course Description

Advanced FPGA Implementation tackles the most sophisticated aspects of the ISE® design suite and Xilinx hardware. Labs provide hands-on experience in this two-day training and cover the Xilinx Synthesis Technology (XST) tools.

This course requires the *Essentials of FPGA Design* and *Designing for Performance* courses as prerequisites. An intermediate knowledge of Verilog or VHDL is strongly recommended as is at least six months of design experience with Xilinx tools and FPGAs. The lecture material in this course covers the ISE tools and the 7 series FPGAs.

Level – FPGA 4

Course Duration – 2 days

Price – $1,600 or 16 Xilinx Training Credits

Course Part Number – FPGA33000-ILT

Who Should Attend? – Engineers who seek advanced training in using Xilinx tools to improve FPGA performance and utilization while also increasing productivity

Prerequisites

- *Essentials of FPGA Design*
- *Designing for Performance*
- Intermediate knowledge of Verilog or VHDL is strongly recommended
- At least six months of design experience with Xilinx tools and FPGAs

Software Tools

- Xilinx ISE Design Suite: Logic or System Edition 14.7

Hardware

- Architecture: Xilinx 7 series FPGAs*

* This course focuses on the 7 series FPGA architectures.

** Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Create and edit a User Constraint File (UCF)
- Identify the I/O timing constraints and design modifications required for source-synchronous and system-synchronous interfaces
- Implement designs via the Tcl command line
- Use the PlanAhead™ tool to create area constraints
- Use design preservation techniques to simplify design ripple effects
- Change signals of interest in the ChipScope™ Pro tool for board-level debugging using the FPGA Editor

Course Outline

- Introduction
- **Lab 1:** Timing Closure Review
- UCF Editing
- **Lab 2:** UCF Editing
- Advanced I/O Timing
- **Lab 3:** Advanced I/O Timing
- Tcl Scripting
- **Lab 4:** Tcl Scripting
- Floorplanning an Effective Layout
- **Lab 5:** Floorplanning
- Design Preservation Techniques
- **Lab 6:** Design Preservation
- FPGA Editor: Viewing and Editing a Routed Design
- **Lab 7:** Advanced FPGA Editor

Lab Descriptions

- **Lab 1:** Timing Closure Review – Use the Constraints Editor to enter timing constraints.
- **Lab 2:** UCF Editing – Write constraints directly into a UCF file to guide the performance results of implementation.
- **Lab 3:** Advanced I/O Timing – Compose timing constraints for source-synchronous and system-synchronous I/O interfaces. Analyze the timing and determine changes to optimize the interface timing.
- **Lab 4:** Tcl Scripting – Write ISE tool control commands in Tcl script files to create a project and implement the design. Explore how the Tcl interface is integrated with the Project Navigator tool.
- **Lab 5:** Floorplanning – Implement a design by using floorplanned constraints to improve the timing results over a design without floorplanning.
- **Lab 6:** Advanced FPGA Editor – Use the FPGA Editor to view and edit a design. Rapidly locate and swap signals of interest for ChipScope Pro tool cores.

Register Today

Morgan Advanced Programmable Systems, Inc. (MAPS, Inc.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota and Wisconsin.

Visit **morgan-aps.com/training**, for full course schedule and training information.

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

MAPS Inc. Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- MAPS may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.

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