Zynq UltraScale+ MPSoC for the Hardware Designer

Embedded Hardware 3

EMBD-ZUPHW-ILT (v1.0)

Course Specification

Course Description

This one-day course is structured to provide hardware designers with an overview of many of the capabilities and support for the Zynq® UltraScale+™ MPSoC family from a hardware architectural perspective.

Level – Embedded Hardware 3

Course Duration – 1 day

Price – $800 or 8 Xilinx Training Credits

Course Part Number – EMBD-ZUPHW-ILT

Who Should Attend? – Hardware designers interested in understanding the architecture and capabilities of the Zynq UltraScale+ MPSoC device.

Prerequisites

- Suggested: Understanding of the Zynq-7000 architecture
- Basic familiarity with embedded software development using C (to support testing of specific architectural elements)

See also

- Zynq UltraScale+ MPSoC for the System Architect
- Embedded Design with PetaLinux Tools

Software Tools

- Vivado® Design Suite 2018.1
  - May require special Zynq UltraScale+ MPSoC family license
- Hardware emulation environment:
  - VirtualBox
  - QEMU
  - Ubuntu desktop
  - PetaLinux

Hardware

- Host computer for running the above software*

* This course focuses on the Zynq UltraScale+ MPSoC architecture. This version of the class does not use a physical board, but rather a local emulation environment and the Vivado Design Suite.

** Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Enumerate the key elements of the application processing unit (APU) and real-time processing unit (RPU)
- List the various power domains and how they are controlled
- Describe the connectivity between the processing system (PS) and programmable logic (PL)
- Utilize QEMU to emulate hardware behavior

Course Outline

- Zynq UltraScale+ MPSoC Application Processing Unit {Lectures, Lab}
- Zynq UltraScale+ MPSoC HW-SW Virtualization {Lectures, Demo, Lab}
- Zynq UltraScale+ MPSoC Real-Time Processing Unit {Lectures, Demo, Lab}
- QEMU {Lectures, Demos}
- Zynq UltraScale+ MPSoC Booting {Lectures, Lab}
- First Stage Boot Loader {Lecture, Demo}
- Zynq UltraScale+ MPSoC Video {Lectures}
- Zynq UltraScale+ MPSoC System Protection {Lectures}
- Zynq UltraScale+ MPSoC Clocks and Resets {Lectures, Demos}
- AXI {Lectures, Demo, Lab}
- Zynq UltraScale+ MPSoC PMU {Lectures, Lab}

Topic Descriptions

- Zynq UltraScale+ MPSoC Application Processing Unit – Introduction to the members of the APU, specifically the Cortex™-A53 processor and how the cluster is configured and managed.
- Zynq UltraScale+ MPSoC HW-SW Virtualization – Covers the hardware and software elements of virtualization. The lab demonstrates how hypervisors can be used.
- Zynq UltraScale+ MPSoC Real-Time Processing Unit – Introduction to the various elements within the RPU and different modes of configuration.
- QEMU – Introduction to the Quick Emulator, which is the tool used to run software for the Zynq UltraScale+ MPSoC device when hardware is not available.
- Zynq UltraScale+ MPSoC Booting – How to implement the embedded system, including the boot process and boot image creation.
- First Stage Boot Loader – Introduction to the FSBL, its importance, and how it can be implemented.
- Zynq UltraScale+ MPSoC Video – Introduction to video, video codecs, and the Video Codec Unit available in the Zynq UltraScale MPSoC.
- Zynq UltraScale+ MPSoC System Protection – Covers all the hardware elements that support the separation of software domains.
- Zynq UltraScale+ MPSoC Clocks and Resets – Overview of clocking and reset, focusing more on capabilities than specific implementations.
- AXI – Understanding how the PS and PL connect enables designers to create more efficient systems.
- Zynq UltraScale+ MPSoC PMU – Overview of the PMU and the power-saving features of the device.

Register Today

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