



dvanced Programmable Systems

## EMBD-ZUPHW (v1.0)

## **Course Description**

This course provides hardware designers with an overview of the capabilities and support for the Zynq® UltraScale+™ MPSoC family from a hardware architectural perspective.

The emphasis is on:

- Identifying the key elements of the application processing unit (APU) and real-time processing unit (RPU)
- Reviewing the various power domains and their control structure
- Illustrating the processing system (PS) and programmable logic (PL) connectivity
- Utilizing QEMU to emulate hardware behavior

#### What's New for 2021.2

All labs have been updated to the latest software versions

Level – Embedded Hardware 3

#### **Course Details**

- 2 days live instructor led training (online or in person)
  - 30 lectures
  - 6 labs
  - 7 ILT demos
- Price \$1,600 or 16 Xilinx Training Credits

Course Part Number – EMBD-ZUPHW

Who Should Attend? – Hardware designers interested in understanding the architecture and capabilities of the Zynq UltraScale+ MPSoC device.

#### Prerequisites

 Basic familiarity with embedded software development using C (to support testing of specific architectural elements)

#### Software Tools

- Vivado® Design Suite 2021.2
- Vitis<sup>™</sup> unified software platform 2021.2
- Hardware emulation environment:
  - VirtualBox (We don't use it as it is too slow)
  - QEMU (We don't use it as running on hardware is superior)
  - Ubuntu desktop (We have it installed natively for faster builds)

# PetaLinux Hardware

Zynq UltraScale+ MPSoC ZCU104 board\*

\* This course focuses on the Zynq UltraScale+ MPSoC architecture. Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Enumerate the key elements of the application processing unit (APU) and real-time processing unit (RPU)
- List the various power domains and how they are controlled
- Describe the connectivity between the processing system (PS) and programmable logic (PL)
- Utilize QEMU to emulate hardware behavior

## Zynq UltraScale+ MPSoC for the Hardware Designer

Embedded Hardware 3

## Course Specification

## **Course Outline**

#### Day 1

#### Application Processing Unit

Introduction to the members of the APU, specifically the Cortex<sup>TM</sup>-A53 processor and how the cluster is configured and managed. {Lectures, Lab}

### HW-SW Virtualization

Covers the hardware and software elements of virtualization. The lab demonstrates how hypervisors can be used. {Lectures, Demo, Lab}

#### Real-Time Processing Unit

Focuses on the real-time processing module (RPU) in the PS, which is comprised of a pair of Cortex processors and supporting elements. {Lectures, Demo, Lab}

#### QEMU

Introduction to the Quick Emulator, which is the tool used to run software for the Zynq UltraScale+ MPSoC device when hardware is not available. {Lectures, Demos}

#### Booting

How to implement the embedded system, including the boot process and boot image creation. {Lectures, Lab}

#### First Stage Boot Loader

Demonstrates the process of developing, customizing, and debugging this mandatory piece of code. {Lecture, Demo}

#### Day 2 Video

Introduction to video, video codecs, and the video codec unit available in the Zyng UltraScale MPSoC. {Lectures}

- System Protection
   Covers all the hardware elements that support the separation of software domains. {Lectures}
- Clocks and Resets

Overview of clocking and reset, focusing more on capabilities than specific implementations. {Lectures, Demos}

AXI

Understanding how the PS and PL connect enables designers to create more efficient systems. {Lectures, Demo, Lab}

#### Power Management

Overview of the PMU and the power-saving features of the device. {Lectures, Lab}

## **Register Today**

Morgan Advanced Programmable Systems, Inc. (Morgan A.P.S.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota, and Wisconsin.

Visit morgan-aps.com/training, for full course schedule and training information.

## Morgan

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

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## Zyng UltraScale+ MPSoC for the Hardware Designer

Embedded Hardware 3

### **Course Specification**

### Student Cancellation Policy

- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class. Student cancellations must be sent here.

## Morgan A.P.S. Course Cancellation Policy

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.

## Online training with real hardware

During the Covid-19 period, some companies do not allow their staff to participate in live in-person training.

- Consequently, Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person...for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your Xilinx based device quickly and efficiently.

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