SDSoC Development Environment and Methodology

Embedded 2

EMBD-SDSOC-ILT (v1.0)

Course Specification

Course Description

This one-day course is structured to help designers new to the SDSoC™ development environment to quickly understand the full "end-user" tool flow to create accelerated systems. The focus is on utilizing the tools to accelerate an existing design at the system architecture level, not on the optimization of the accelerator microarchitectures.

Several optional modules are provided to quickly provide students with the necessary background on both hardware and software.

Level – Embedded 2

Course Duration – 1 day

Price – $800 or 8 Xilinx Training Credits

Course Part Number – EMBD-SDSOC-ILT

Who Should Attend? – Anyone interested in quickly adding hardware acceleration to a software system.

Prerequisites

- Understanding of Zynq®-7000 architecture (with emphasis on ACP, HP ports, and internal routing)
- Comfort with the C programming language
- Familiarity with the Vivado® Design Suite, Vivado HLS tool, and Xilinx SDK

Recommended

- Zynq SoC System Architecture course
- C-based Design: High-Level Synthesis with the Vivado HLx Tool course
- Advanced SDSoC Development Environment and Methodology course

Software Tools

- SDx™ development environment 2017.4

Hardware

- Architecture: Zynq-7000 All Programmable SoC*
- Demo board: Zynq-7000 All Programmable SoC ZC702 or ZedBoard*

* This course focuses on the Zynq-7000 All Programmable SoC.

** Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Identify candidate functions for hardware acceleration by using the TCF profiling tool
- Use the System Debugger's capabilities to control the execution flow and examine memory and variables during a debug session
- Move designated software functions to hardware and estimate the performance of the accelerator and the effect on the entire system
- Use the hardware/software event trace to understand the performance of an application given the workload, hardware/software partitioning, and system design choices

Course Outline

- Zynq AP SoC Architecture Support for Accelerators [Optional]
- Software Overview [Optional]
- Introduction to the SDSoC Tool {Lecture}
- SDSoC Tool Flow {Lecture, Demo, Lab}
- Application Debugging {Lecture, Demo, Lab}
- Application Profiling {Lecture, Demo, Lab}
- Understanding Estimations in the SDSoC Tool {Lecture, Demo, Lab}
- QEMU Emulation {Lab}
- Hardware/Software Event Tracing {Lecture, Lab}

Topic Descriptions

- Zynq AP SoC Architecture Support for Accelerators [Optional] – Discusses the relevant aspects of the Zynq All Programmable SoC architecture for accelerator design. The focus is on AXI ports and protocols, system latency, and memory utilization.
- Software Overview [Optional] – Provides a thorough understanding of how the integrated design environment works, including how the compiler and linker behave, basics of makefiles, DMA usage, and variable scope.
- Introduction to the SDSoC Tool {Lecture} – Introduces the purpose, underlying structures, and basic functionality of the SDSoC development environment.
- SDSoC Tool Flow {Lecture, Demo, Lab} – Explains the complete development flow of the SDSoC integrated development environment (IDE).
- Application Debugging {Lecture, Demo, Lab} – Through the use of the System Debugger, students will learn how to follow the control flow in an executing application and see the effects of the code on memory to successfully debug software issues.
- Application Profiling {Lecture, Demo, Lab} – Profiling is the process that identifies how the processor is spending its time. Through profiling, the user can quickly identify which functions must be optimized or moved to hardware to satisfy the performance requirements.
- Understanding Estimations in the SDSoC Tool {Lecture, Demo, Lab} – Once a function is moved to hardware, questions remain: Will the accelerator fit in hardware? Will it fun fast enough? Estimations can provide the answers.
- QEMU Emulation {Lab} – Describes how to use the emulation feature in the SDx IDE.
- Hardware/Software Event Tracing {Lecture, Lab} – Hardware/software event tracing helps users understand the performance of their application given the workload, hardware/software partitioning, and system design choices. Such information helps the user to optimize and improve system implementation.

Register Today

Morgan Advanced Programmable Systems, Inc. (MAPS, Inc.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota and Wisconsin.

Visit **morgan-aps.com/training**, for full course schedule and training information.

Morgan Advanced Programmable Systems

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

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- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

MAPS Inc. Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
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