

Course Description

Learn how to develop new applications written in OpenCL, C/C++, and RTL in the SDAccel™ development environment for use on Xilinx FPGAs. Porting existing applications is also covered.

This course also demonstrates how to debug and profile OpenCL code using the SDAccel development environment. In addition, you will also learn how to maximize performance and efficiently utilize FPGA resources.

Level – SDx 2

Course Duration – 2 days

Price – \$1,600 or 16 Xilinx Training Credits

Course Part Number – EMBD-OCLSDA

Who Should Attend? – Software and hardware developers who want to develop OpenCL, C/C++, and RTL applications in the SDAccel development environment.

Prerequisites

- Basic knowledge of C/C++

Software Tools

- SDAccel development environment and common build tools

Hardware

- Architecture: 7 series, UltraScale, UltraScale+

Follow-up training

- [Developing AWS F1 Applications Using the SDAccel Environment](#) course

* This course focuses on the 7 series, UltraScale, and UltraScale+ architectures. ** Check with [Morgan Advanced Programmable Systems, Inc.](#) for the specifics of the in-class lab board or other customizations.

Note: This class will be updated soon to a later version of the SDAccel tools. This specification sheet is a placeholder.

After completing this comprehensive training, you will have the necessary skills to:

- Identify parallel computing applications suitable for accelerating on FPGAs
- Discover how the FPGA architecture lends itself to parallel computing
- Write OpenCL programs for FPGAs
- Examine the OpenCL execution model
- Analyze the OpenCL memory model
- Profile and debug OpenCL code using the SDAccel development environment
- Discover how to maximize performance in FPGA fabric
- Efficiently utilize FPGA memory resources
- Utilize the SDAccel development environment
- Rapidly develop FPGA applications using OpenCL
- Port programs written in OpenCL for CPUs or GPUs to Xilinx FPGAs

Course Outline

Day 1

- Introduction to OpenCL
- Comparison of CPU, GPU, and FPGA Architectures
- OpenCL Support for Xilinx FPGAs
- FPGA Hardware Details
- Introduction to the OpenCL API

- **Lab 1:** Creating an OpenCL Program from Scratch
- OpenCL Execution Model
- **Lab 2:** Vector Addition
- Memory Hierarchy
- Profiling and Debugging
- **Lab 3:** Pi by Monte Carlo Processes
- Optimization
- **Lab 4:** Maximizing Performance
- **Lab 5:** Optimizing Kernels

Day 2

- Using the SDAccel Development Environment: Coding, Compiling, Emulating, Profiling, and Debugging
- **Lab 6:** Profiling and Debugging Using the SDAccel Development Environment GUI
- Using Existing C/C++ Code as Kernels in OpenCL
- **Lab 7:** Optimizing C/C++ Code for OpenCL
- RTL IP as Kernels in OpenCL
- **Lab 8:** Using an RTL Kernel

Lab Descriptions

- **Lab 1:** Creating an OpenCL Program from Scratch – Provides an overview of OpenCL API, memory transfers, and kernel enqueue operations.
- **Lab 2:** Vector Addition – Learn how to execute parallel kernels.
- **Lab 3:** Pi by Monte Carlo Processes – Implement the Pi by Monte Carlo processes.
- **Lab 4:** Maximizing Performance – Use vector data types and increase bandwidth.
- **Lab 5:** Optimizing Kernels – Use Loop Unrolling and Loop Pipelining.
- **Lab 6:** Profiling and Debugging Using the SDAccel Development Environment GUI – Learn how to use interactive programming tools to improve performance and squash bugs.
- **Lab 7:** Optimizing C/C++ Code for OpenCL – Convert existing C/C++ code into a kernel that can be used by OpenCL
- **Lab 8:** Using an RTL Kernel – Learn how to use existing, highly optimized IP in a new OpenCL application.

Demo Descriptions

- Demo 1: SDAccel Development Environment Flow Overview – Provides an overview of the SDAccel tool flow, such as creating a project, compiling, emulating, and profiling.
- Demo 2: Memory Optimization – Learn to improve the performance of the kernel.

Register Today

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Visit morgan-aps.com/training, for full course schedule and training information.



You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent [here](#).

MAPS Inc. Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- MAPS may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is MAPS responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us [here](#).