Embedded Systems Design

Embedded Hardware 3

EMBD-HW (v1.0)

Course Specification

Course Description

Learn general embedded concepts, tools, and techniques using the Vivado® Design Suite and Vitis™ unified software platform.

The emphasis is on:

- Designing, expanding, and modifying embedded systems utilizing the features and capabilities of the Zynq® System on a Chip (SoC), Zynq UltraScale+™ MPSoC, or MicroBlaze™ soft processor
- Adding and simulating AXI-based peripherals using bus functional model (BFM) simulation

What's New for 2021.2

- All labs have been updated to the latest software versions

Level – Embedded Hardware 3

Course Details

- 2 days live instructor led training (in person or online)
  - 17 lectures
  - 8 labs
  - 6 ILT demos

Price – $1,600 or 16 Xilinx Training Credits

Course Part Number – EMBD-HW

Who Should Attend? – Engineers who are interested in developing embedded systems with the Xilinx Zynq SoC, Zynq UltraScale+ MPSoC, and/or MicroBlaze soft processor core

Prerequisites

- FPGA design experience
- Completion of the Designing FPGAs Using the Vivado Design Suite 1 course or equivalent knowledge of Xilinx Vivado software implementation tools
- Basic understanding of C programming
- Basic understanding of microprocessors
- Some Verilog of VHDL modeling experience

Software Tools

- Vivado Design Suite 2021.2
- Vitis unified software platform 2021.2

Hardware

- Architectures: Zynq-7000 SoC (Cortex™-A9 processor), Zynq UltraScale+ MPSoC (Cortex-A53 and Cortex-R5 processors), and MicroBlaze processor*
- Demo board: Zynq UltraScale+ MPSoC ZCU104 or Versal® ACAP VCK190 board*

* This course focuses on the Zynq-7000 SoC and Zynq UltraScale+ MPSoC architectures. Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the various tools that encompass a Xilinx embedded design
- Rapidly architect an embedded system containing a Cortex-A9/A53/R5 or MicroBlaze processor using the Vivado IP integrator and Customization Wizard
- Develop software applications utilizing the Vitis unified software platform
- Create and integrate an IP-based processing system component in the Vivado Design Suite
- Design and add a custom AXI interface-based peripheral to the embedded processing system
- Simulate a custom AXI interface-based peripheral using verification IP (VIP)

Course Outline

Day 1

- **Embedded UltraFast Design Methodology**
  Outlines the different elements that comprise the Embedded Design Methodology. {Lecture, Demo}
- **Overview of Embedded Hardware Development**
  Overview of the embedded hardware development flow. {Lecture, Demo}
- **Driving the IP Integrator Tool**
  Describes how to access and effectively use the IPI tool. {Lecture, Lab}
- **Overview of Embedded Software Development**
  Reviews the process of building a user application. {Lecture}
- **Driving the Vitis Software Development Tool**
  Introduces the basic behaviors required to drive the Vitis tool to generate a debuggable C/C++ application. {Lecture, Lab}
- **AXI: Introduction**
  Introduces the AXI protocol. {Lecture}
- **AXI: Variations**
  Describes the differences and similarities among the three primary AXI variations. {Lecture}
- **AXI: Transactions**
  Describes different types of AXI transactions. {Lecture, Demo, Lab}
- **Introduction to Interrupts**
  Introduces the concept of interrupts, basic terminology, and generic implementation. {Lecture}
- **Interrupts: Hardware Architecture and Support**
  Reviews the hardware that is typically available to help implement and manage interrupts. {Lecture}

Day 2

- **AXI: Connecting AXI IP**
  Describes the relationships between different types of AXI interfaces and how they can be connected to form hierarchies. {Lecture, Demo}
- **Creating a New AXI IP with the Wizard**
  Explains how to use the Create and Import Wizard to create and package an AXI IP. {Lecture, Lab}
- **AXI: BFM Simulation Using Verification IP**
  Describes how to perform BFM simulation using the Verification IP. {Lecture, Lab}
- **MicroBlaze Processor Architecture Overview**
  Overview of the MicroBlaze microprocessor architecture. {Lecture, Lab}
- **MicroBlaze Processor Block Memory Usage**
  Highlights how block RAM can be used with the MicroBlaze processor. {Lecture}

© 2022 Xilinx, Inc. All rights reserved. All Xilinx trademarks, registered trademarks, patents, and disclaimers are as listed at http://www.xilinx.com/legal.htm.
All other trademarks and registered trademarks are the property of their respective owners. All specifications are subject to change without notice.

- **Zynq-7000 SoC Architecture Overview**
  Overview of the Zynq-7000 SoC architecture. {Lecture, Demo, Lab}
- **Zynq UltraScale+ MPSoC Architecture Overview**
  Overview of the Zynq UltraScale+ MPSoC architecture. {Lecture, Demo, Lab}

Register Today

Morgan Advanced Programmable Systems, Inc. (Morgan A.P.S.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota, and Wisconsin.

Visit **morgan-aps.com/training**, for full course schedule and training information.

Morgan Advanced Programmable Systems

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

Morgan A.P.S. Course Cancellation Policy

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.

Online training with real hardware

During the Covid-19 period, some companies do not allow their staff to participate in live in-person training.

- Consequently, Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.

Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your Xilinx based device quickly and efficiently.

© 2022 Xilinx, Inc. All rights reserved. All Xilinx trademarks, registered trademarks, patents, and disclaimers are as listed at http://www.xilinx.com/legal.htm.
All other trademarks and registered trademarks are the property of their respective owners. All specifications are subject to change without notice.