Developing AWS F1 Applications Using the SDAccel Environment

EMBD 2

EMBD-AWS-ILT (v1.0)

Course Specification

Course Description

This one-day course is structured to help designers new to the Amazon Web Services (AWS) F1 instance quickly understand the complete flow of design generation for AWS F1. The focus is on utilizing the tools to accelerate a design at the system architecture level and the optimization of the accelerators.

Level – EMBD 2

Course Duration – 1 day

Price – $800 or 8 Xilinx Training Credits

Course Part Number – EMBD-AWS-ILT

Who Should Attend? – Anyone interested in quickly adding hardware acceleration to a software system.

Prerequisites

- Basic knowledge of Xilinx FPGA architecture
- Comfort with the C programming language
- Familiarity with OpenCL™ API programming
  - Developing and Optimizing Applications Using the OpenCL Framework for FPGAs course or equivalent

Software Tools

- SDx™ development environment 2017.4

Hardware

- Architecture: AWS-VU9P-F1 (Virtex® UltraScale+™ VU9 FPGA)

* Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the Amazon Web Services (AWS) F1 instance development flow with the SDAccel™ development environment
- Explain how the SDx™ development environment helps the software developer to focus on applications
- Create kernels from C, C++, OpenCL, or RTL IP
- Describe the RTL kernel interface requirements
- Create a kernel with the RTL Kernel Wizard

Course Outline

- Introduction to the AWS F1 Instance and the SDAccel Environment {Lecture}
- Understanding the AWS F1 Hardware and Software Stacks {Lecture}
- Introduction to the SDAccel Environment and OpenCL Framework {Lecture}
- SDx Tools Overview {Lecture}
- Creating Kernels and Compiling the Amazon FPGA Image {Lecture}
- Setting Up an AWS F1 Instance {Lecture, Lab}
- Running an Example Design Using the Makefile Flow { Lab}
- Running an Example Design Using the GUI Flow {Lab}
- Profiling and Optimizing an F1 Accelerator {Lab}
- Using the RTL Kernel Wizard to Reuse Existing IP as F1 Accelerators {Lecture, Lab}

Topic Descriptions

- Introduction to the AWS F1 Instance and the SDAccel Environment {Lecture} – Describes the AWS F1 instance, the benefits of using the F1 instance, and the AWS F1 development flow.
- Understanding the AWS F1 Hardware and Software Stacks {Lecture} – Explains the hardware and software stacks of the AWS F1 platform and explains how they work together to provide an acceleration solution.
- Introduction to the SDAccel Environment and OpenCL Framework {Lecture} – Explains how software engineers and application developers can benefit from the SDAccel™ development environment and Open Computing Language (OpenCL™) framework.
- SDx Tools Overview {Lecture} – Describes the elements of the development flow, such as software emulation, hardware emulation, and system run as well as debugging support for the host code and kernel code.
- Creating Kernels and Compiling the Amazon FPGA Image {Lecture} – Explains the steps required to create FPGA kernels, assemble the FPGA program, and compile the Amazon FPGA Image (AFI).
- Setting Up an AWS F1 Instance {Lecture, Lab} – Describes how to set up an AWS account, configure the instance, and set up the SDAccel development environment.
- Running an Example Design Using the Makefile Flow { Lab} – Walks through running an example design on AWS F1 using the makefile flow.
- Running an Example Design Using the GUI Flow {Lab} – Walks through running an example design on AWS F1 using the GUI flow.
- Profiling and Optimizing an F1 Accelerator {Lab} – Details using the SDAccel development environment to create, profile, and optimize an F1 accelerator.
- Using the RTL Kernel Wizard to Reuse Existing IP as F1 Accelerators {Lecture, Lab} – Describes how the SDAccel environment provides RTL kernel developers with a framework to integrate their hardware functions into an application running on a host PC connected to an FPGA via a PCIe® interface.

Register Today

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Visit **morgan-aps.com/training**, for full course schedule and training information.

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

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- Student cancellations must be sent here.

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- In the event of cancellation, live on-line training may be offered as a substitute.
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