# Advanced Embedded Systems Software Design

Embedded Software 4

EMBD-ADVSW-ILT (v1.0)

**Course Specification**

## Course Description

This course will help software engineers make full use of the components available in the Zynq® All Programmable System on a Chip (SoC) processing system (PS). This course covers advanced Zynq All Programmable SoC topics for the software engineer, including advanced boot methodology, the NEON co-processor, programming PS system-level function control registers, the general interrupt controller, the DMA, Ethernet, and USB controllers, and the various low-speed peripherals included in the Zynq All Programmable SoC processing system.

**Level** – Embedded Software 4

**Course Duration** – 1 day

**Price** – $800 or 8 Xilinx Training Credits

**Course Part Number** – EMBD-ADVSW-ILT

**Who Should Attend?** Software design engineers interested in fully using the Zynq extensible processing platform

**Prerequisites**

- *Embedded Systems Software Design* course
- C or C++ programming experience
- Conceptual understanding of embedded processing systems, including device drivers, interrupt routines, Xilinx Standalone library services, user applications, and boot loader operation
- Experience developing software for embedded processor applications

**Software Tools**

- Vivado® Design or System Edition 2017.3

**Hardware**

- Architecture: Zynq-7000 All Programmable SoC*
- Demo board: Zynq-7000 All Programmable SoC ZC702 or ZedBoard*

* This course focuses on the Zynq-7000 All Programmable SoC.

** Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Implement an effective Zynq All Programmable SoC boot design methodology
- Create an appropriate FSBL image for flash
- Identify advanced Cortex™-A9 processor services for fully utilizing the capabilities of the Zynq All Programmable SoC
- Analyze the operation and capabilities of the DMA controller in the Zynq All Programmable SoC
- Examine the various Standalone library services and performance capabilities of the Ethernet and USB controllers in the Zynq All Programmable SoC
- Describe the Standalone library services available for low-speed peripherals that are contained in the Zynq All Programmable SoC PS

## Course Outline

- Booting
  - Overview {Lecture, Lab}
  - Boot Memory Technologies {Lecture}
  - Flow {Lecture}
  - PS Processors {Lecture, Lab}
  - PL {Lecture, Lab}
  - Secure Boot {Lecture}
  - FSBL {Lecture, Demo}
- General Interrupt Controller {Lecture}
- Processor Caching and SCLR {Lecture}
- NEON Co-Processing {Lecture}
- DMA
  - Introduction and Features {Lecture}
  - Block Design and Interrupts {Lecture}
  - Read and Write {Lecture, Lab}
- High-Speed Peripherals
  - Gigabit Ethernet {Lecture, Lab}
  - USB {Lecture}
- Low-Speed Peripherals
  - Overview {Lecture, Lab}
  - UART {Lecture, Demo}
  - CAN {Lecture, Demo}
  - I2C {Lecture}
  - SPI {Lecture}
  - SD/SDIO {Lecture}

## Topic Descriptions

- Booting
  - Overview – Introduces the main points to how booting a processor is handled in Zynq All Programmable devices and MicroBlaze processors.
  - Boot Memory Technologies – Introduces the main points of the memories that can be booted or executed from.
  - Flow – Provides a low-level view of the booting process.
  - PS Processors – Introduces the concepts behind a single-core boot, a dual-core boot, and symmetric or asymmetric processing.
  - PL – Introduces the concepts behind configuring the PL at boot.
  - Secure Boot – Introduces the concepts behind secure booting.
  - FSBL – Introduces the First Stage Boot Loader (FSBL).
- General Interrupt Controller – Introduces the general interrupt controller (GIC), its features, and some examples of its use.
- Processor Caching and SCLR – Introduces the concepts behind processing caching and the System-Level Control Register.
- NEON Co-Processing – Introduces the concepts behind the NEON co-processor.
- DMA
  - Introduction and Features – Introduces the direct memory access controller.
  - Block Design and Interrupts – Introduces the DMA block design and the DMA interrupts.
  - Read and Write – Introduces the concepts behind DMA reading and writing.
- High-Speed Peripherals
  - Gigabit Ethernet – Introduces the Gigabit Ethernet high-speed peripheral.
  - USB – Introduces the USB high-speed peripheral.
- Low-Speed Peripherals
  - Overview – Introduces the low-speed peripherals in the Zynq All Programmable SoC.
  - UART – Introduces the UART low-speed peripheral.
  - CAN – Introduces the CAN low-speed peripheral.
  - I2C – Introduces the I2C low-speed peripheral.
  - SPI – Introduces the SPI low-speed peripheral.
  - SD/SDIO – Introduces the SD/SDIO low-speed peripheral.

## Register Today

Morgan Advanced Programmable Systems, Inc. (MAPS, Inc.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota and Wisconsin.

Visit **morgan-aps.com/training**, for full course schedule and training information.

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

## Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

## MAPS Inc. Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- MAPS may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is MAPS responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.