Zynq Master Training for Experienced FPGA Engineers

Embedded Architect 3

EMBD-33040-ILT (v1.0)

Course Specification

Course Description

Xilinx Zynq®-7000 provides a new level of performance in creating custom high-performance systems on a chip (SoC). This intensive cross functional training is designed to bring FPGA designers up to speed on developing embedded systems using the Vivado® Design Suite. The features and capabilities of the Zynq® System on a Chip (SoC), the Zynq UltraScale+™ MPSoC, and the MicroBlaze™ soft processor are covered in lectures, demonstrations, and labs, along with general embedded concepts, tools, and techniques. The hands-on labs provide students with experience designing, expanding, and modifying an embedded system, including adding custom AXI-based peripheral IP, and writing simple device drivers, and how everything relates to each other in the context of the Xilinx design tools.

The course details the individual components that comprise the PS: I/O peripherals, timers, caching, PS and PL based DMA, interrupt, and memory controllers. Emphasis is placed on effective access and usage of the PS DDR controller based on your project's needs, and the advantages and costs associated with implementing functions in the PS or the PL.

Level – Embedded Hardware/ Architect 3

Course Duration – 3 days

Price – $2,400 or 24 Xilinx Training Credits

Course Part Number – EMBD-33040-ILT

Who Should Attend? – Engineers who are interested in developing embedded systems with the Xilinx Zynq SoC, Zynq UltraScale+ MPSoC, and/or MicroBlaze soft processor core, and System architects who are interested in architecting a system on a chip using the SoC.

Prerequisites

- FPGA design experience
- Completion of the Designing FPGAs Using the Vivado Design Suite 1 course or equivalent knowledge of Xilinx Vivado® software implementation tools
- Basic understanding of C programming, microprocessors
- Some HDL modeling experience helpful

See also

- Zynq SoC System Architecture course
- Zynq UltraScale+ MPSoC for the System Architect course
- Zynq UltraScale+ MPSoC for the Hardware Designer course

Software Tools

- Vivado® Design or System Edition 2019.2

Hardware

- Architectures: Zynq-7000 SoC (Cortex™-A9 processor), Zynq UltraScale+ MPSoC (Cortex-A53 and Cortex-R5 processors), and MicroBlaze processor*
- Demo board: Zynq-7000 SoC ZC702 or ZedBoard*

* This course focuses on the Zynq-7000 SoC and Zynq UltraScale+ MPSoC architectures. This course focuses on the UltraScale and 7 series architectures.

** Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations (e.g., a focus on MicroBlaze, MPSoC, or RFSoC).

After completing this comprehensive training, you will have the necessary skills to:

- Describe the various tools that encompass a Xilinx embedded design
- Rapidly architect an embedded system containing a Cortex-A9/A53/R5 or MicroBlaze processor using the Vivado IP integrator and Customization Wizard
- Develop software applications utilizing the Eclipse-based Software Development Kit (SDK)
- Create and integrate an IP-based processing system component in the Vivado Design Suite
- Design and add a custom AXI interface-based peripheral to the embedded processing system
- Simulate a custom AXI interface-based peripheral using verification IP (VIP)
- Describe the architecture and components that comprise the Zynq SoC processing system (PS)
- Relate a user design goal to the function, benefit, and use of the Zynq SoC
- Effectively select and design an interface between the Zynq PS and programmable logic (PL) that meets project goals
- Analyze the tradeoffs and advantages of performing a function in software versus PL

Course Outline

Day 1

- Zynq All Programmable SoC Overview
- Inside the Application Processor Unit (APU)
- Processor Input/Output Peripherals
- **Lab 1: Extended student/Instructor demonstration and follow along lab:** Investigate AXI bus, AXI interconnect, DMA performance, and tips and tricks of Vivado Logic Analyzer. Benchmark DMA performance. Understand relationship between settings in IP Integrator and SDK drivers/headers/APIs.

Day 2

- Formal Introduction to AXI
- Zynq All Programmable SoC PS-PL interface
- Programable SoC
- Zynq All Programmable SoC Booting
- Zynq All Programmable SoC Memory resources
- **Lab 2**: Debugging on the Zynq All Programmable SoC, PS and PL simultaneously

Day 3

- Meeting Performance Goals
- Embedded Design Overview
- IP and the PS Configuration Wizard
- **Lab 3**: Extended student/Instructor Demonstration and follow along lab. Integrating a simple, highly illustrative custom IP into AXI, with cross functional troubleshooting. Troubleshoot using SDK, Vivado XSIM, Vivado Logic Analyzer, and/or digital oscilloscope. Custom VHDL and lab instructions included
- Optional (if time permits): constructing and using a Finite Impulse Response DSP subsystem with data movers, including software drivers.

In addition to the above, you will receive the printed materials and labs that can be self-studied (SS) after class:

SS Day 1

- Embedded UltraFast Design Methodology – Outlines the different elements that comprise the Embedded Design Methodology.
- Overview of Embedded Hardware Development – Overview of the embedded hardware development flow.
- Driving the IP Integrator Tool – Describes how to access and effectively use the IPI tool.
- Overview of Embedded Software Development – Reviews the process of building a user application.

- Driving the SDK Tool – Introduces the basic behaviors required to drive the SDK tool to generate a C/C++ application that can be debugged.
- AXI: Introduction – Introduces the AXI protocol.
- AXI: Variations – Describes the differences and similarities among the three primary AXI variations.
- AXI: Transactions – Describes different types of AXI transactions.
- Introduction to Interrupts – Introduces the concept of interrupts, basic terminology, and generic implementation.
- Interrupts: Hardware Architecture and Support – Reviews the hardware that is typically available to help implement and manage interrupts.

SS Day 2

- AXI: Connecting AXI IP – Describes the relationships between different types of AXI interfaces and how they can be connected to form hierarchies.
- Using the Create and Import Wizard to Create a New AXI IP – Explains how to use the Create and Import Wizard to create and package an AXI IP.
- AXI: BFM Simulation Using Verification IP – Describes how to perform BFM simulation using the Verification IP.
- MicroBlaze Processor Architecture Overview – Overview of the MicroBlaze microprocessor architecture.
- MicroBlaze Processor Block Memory Usage – Highlights how block RAM can be used with the MicroBlaze processor.
- Zynq-7000 SoC Architecture Overview – Overview of the Zynq-7000 SoC architecture.
- Zynq UltraScale+ MPSoC Architecture Overview – Overview of the Zynq UltraScale+ MPSoC architecture.

SS Day 3

- Overview – Provides a general overview of the Zynq SoC.
- Application Processor Unit (APU) – Explores the individual components that comprise the APU.
- Neon Co-Processor – Describes the Neon co-processor that is the companion to each Cortex-A9 processor.
- Input/Output Peripherals – Introduces the components that comprise the IOP block of the Zynq device PS.
- Peripherals
  - Low-Speed: Overview – Introduces the low-speed peripherals in the Zynq SoC.
  - Low-Speed: UART – Introduces the UART low-speed peripheral.
  - Low-Speed: CAN – Introduces the CAN low-speed peripheral.
  - Low-Speed: I2C – Introduces the I2C low-speed peripheral.
  - Low-Speed: SD/SDIO – Introduces the SD/SDIO low-speed peripheral.
  - Low-Speed: GPIO – Introduces the GPIO low-speed peripheral.
  - High-Speed: USB – Introduces the USB high-speed peripheral.
  - High-Speed: Gigabit Ethernet – Introduces the Gigabit Ethernet high-speed peripheral.
- DMA Controller (DMAC) – Explores the operation of the DMAC, which is in the APU.
- DMA
  - Introduction and Features – Introduces the direct memory access controller.
  - Block Design and Interrupts – Introduces the DMA block design and the DMA interrupts.
  - Read and Write – Introduces the concepts behind DMA reading and writing.

SS Day 4

- AXI
  - Introduction – Introduces the AXI protocol.
  - Variations – Describes the differences and similarities among the three primary AXI variations.
  - Transactions – Describes different types of AXI transactions.
- PS-PL Interface – Describes in detail the PS interconnect and how it affects PL architecture decisions.
- Booting – Explains the boot process of the PC and configuration of the PL.
- Memory Resources – Explains the operation of the on-chip (OCM) memory and various memory controllers located in the PS.
- Meeting Performance Goals – Focuses on Zynq device performance, including DDR access from the PL, DMA considerations, and power control and reduction techniques.
- Hardware Design – Discusses the use and configuration of the PS in a hardware design.
- Software Design – Explores the software side of the Zynq device.
- Debugging – Introduces debug tools and methodology on the Zynq SoC.
- Tools and Reference Designs – Describes Xilinx-provided reference design platforms, use cases, and third-party operating systems and tools for the Zynq SoC.

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