DSP Design Using System Generator

DSP 3

DSP-SYSGEN (v1.0)

Course Specification

Course Description

Explore the System Generator tool and gain the expertise needed to develop advanced, low-cost DSP designs.

This course focuses on:

- Implementing DSP functions using System Generator for DSP
- Utilizing design implementation tools
- Verifying through hardware co-simulation

What's New for 2019.2

- Introduction to Model Composer: New block descriptions
- Automatic Code Generation: Additional Model Composer information

Level – DSP 3

Course Duration – – 2 days live instructor led training (in person or online)

Price – $1,600 or 16 Xilinx Training Credits

Course Part Number – DSP-SYSGEN

Who Should Attend? – System engineers, system designers, logic designers, and experienced hardware engineers who are implementing DSP algorithms using the MathWorks MATLAB® and Simulink® software and want to use Xilinx System Generator for DSP design

Prerequisites

- Experience with the MATLAB and Simulink software
- Basic understanding of sampling theory

Software Tools

- Vivado® Design Suite System Edition 2019.2
- Model Composer
- MATLAB with Simulink software R2018a, R2018b, R2019a, R2019b

Hardware

- Architecture: 7 series and UltraScale™ FPGAs
- Demo boards (Provided during training): Kintex®-7 FPGA KC705 board or Kintex UltraScale™ FPGA KCU105 board and Zynq® UltraScale+™ MPSoC ZCU104 board*

* Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the System Generator design flow for implementing DSP functions
- Identify Xilinx FPGA capabilities and how to implement a design from algorithm concept to hardware simulation
- List various low-level and high-level functional blocks available in System Generator
- Run hardware co-simulation
- Identify the high-level blocks available for FIR and FFT designs
- Implement multi-rate systems in System Generator
- Integrate System Generator models into the Vivado IDE
- Design a processor-controllable interface using System Generator for DSP
- Generate IPs from C-based design sources for use in the System Generator environment

Course Outline

Day 1

- Introduction to System Generator
- Simulink Software Basics
- **Lab 1:** Using the Simulink Software
- Basic Xilinx Design Capture
- Demo: System Generator Gateway Blocks
- **Lab 2:** Getting Started with Xilinx System Generator
- Signal Routing
- **Lab 3:** Signal Routing
- Implementing System Control
- **Lab 4:** Implementing System Control

Day 2

- Multi-Rate Systems
- **Lab 5:** Designing a MAC-Based FIR
- Filter Design
- **Lab 6:** Designing a FIR Filter Using the FIR Compiler Block
- System Generator, Vivado Design Suite, and Vivado HLS Integration
- **Lab 7:** System Generator and Vivado IDE Integration
- DSP Platforms
- **Lab 8:** System Generator and Vivado HLS Tool Integration
- **Lab 9:** AXI4-Lite Interface Synthesis
- Introduction to Model Composer
- Demo: Introduction to Model Composer
- [OPTIONAL]: Importing C/C++ Code to Model Composer
- [OPTIONAL]: Automatic Code Generation Using Model Composer
- [OPTIONAL]: Lab 10: Model Composer and Vivado IDE Integration

Lab Descriptions

- **Lab 1:** Using the Simulink Software – Learn how to use the toolbox blocks in the Simulink software and design a system. Understand the effect sampling rate.
- **Lab 2:** Getting Started with Xilinx System Generator – Illustrates a DSP48-based design. Perform hardware co-simulation verification targeting a Xilinx evaluation board.
- **Lab 3:** Signal Routing – Design padding and unpadding logic by using signal routing blocks.
- **Lab 4:** Implementing System Control – Design an address generator circuit by using blocks and Mcode.
- **Lab 5:** Designing a MAC-Based FIR – Using a bottom-up approach, design a MAC-based bandpass FIR filter and verify through hardware co-simulation by using a Xilinx evaluation board.
- **Lab 6:** Designing a FIR Filter Using the FIR Compiler Block – Design a bandpass FIR filter by using the FIR Compiler block to demonstrate increased productivity. Verify the design through hardware co-simulation by using a Xilinx evaluation board.
- **Lab 7:** System Generator and Vivado IDE Integration – Embed System Generator models into the Vivado IDE.
- **Lab 8:** System Generator and Vivado HLS Tool Integration – Generate IP from a C-based design to use with System Generator.

- **Lab 9:** AXI4-Lite Interface Synthesis – Package a System Generator for DSP design with an AXI4-Lite interface and integrate this packaged IP into a Zynq UltraScale+ MPSoC processor system.
- **Lab 10:** Model Composer and Vivado IDE Integration - Embed a Model Composer model into the Vivado IDE.

Register Today

Morgan Advanced Programmable Systems, Inc. (Morgan A.P.S.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota, and Wisconsin.

Visit **morgan-aps.com/training**, for full course schedule and training information.

Morgan Advanced Programmable Systems

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

Morgan A.P.S. Course Cancellation Policy

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.

Online training with real hardware

During the Covid-19 period, some companies do not allow their staff to participate in live in-person training.

- Consequently, Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your Xilinx based device quickly and efficiently.