C-based HLS Coding for Software Designers

DSP 3

DSP23000-ILT (v1.0)

Course Specification

Course Description

C-based coding is increasingly used for the modeling and high-level synthesis of hardware components. This course provides software engineers with sufficient knowledge of FPGA hardware to efficiently code for high-level synthesis. Learn the high-level synthesis best practices, methodology, and subtleties of C-based coding for hardware modeling, synthesis, and verification.

Level – DSP 3

Course Duration – 1 day

Price – $800 or 8 Xilinx Training Credits

Course Part Number – DSP23000-ILT

Who Should Attend? – Software engineers looking to utilize high-level synthesis

Prerequisites

- C, C++, or System C knowledge
- Software design experience

Software Tools

- Vivado™ System Edition 2012.2

Hardware

- Architecture: Zynq™-7000 All Programmable SoC and 7 series FPGAs*
- Demo board: Not applicable

* This course focuses on the Zynq-7000 All Programmable SoC and 7 series FPGA architectures.

** Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the difference between software programming and hardware design
- Identify the fundamental principles of hardware design
- Model and simulate hardware components using C
- Code hardware components in C for high-level synthesis

Course Outline

- Introduction to Hardware Design for Software Designers
- **Lab 1:** Analyze a Simple Top-Level Hardware Design
- C-based Algorithmic Coding for Hardware
- **Lab 2:** High-Level Synthesis of a C Model
- C-based Test Bench Coding
- **Lab 3:** Creating a C-based Test Bench

Lab Descriptions

- **Lab 1:** Analyze a Simple Top-Level Hardware Design – Analyze a top-level, two-frequency pulse width modulator (PWM) hardware system. Identify and analyze hardware design components, parallel flow, and control.
- **Lab 2:** High-Level Synthesis of C Model – Use various techniques and directives in Vivado HLS to improve design performance. The design under consideration accepts an image in a (custom) RGB format, converts it to the Y'UV color space, and applies a filter to the Y'UV image and converts it back to RGB.
- **Lab 3:** Creating a C-based Test Bench – Develop a verification environment used for testing a C-based design and verification in Vivado HLS. The design under consideration is the same design used in the previous lab, a Y'UV filter.

Register Today

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

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