

Course Description

C-based coding is increasingly used for the modeling and high-level synthesis of hardware components. This course provides hardware engineers with sufficient knowledge of C-programming techniques for Vivado™ HLS to take advantage of Xilinx FPGAs. Learn high-level synthesis best practices, methodology, and subtleties of C-based coding for hardware modeling, synthesis, and verification.

Level – DSP 3

Course Duration – 1 day

Price – \$800 or 8 Xilinx Training Credits

Course Part Number – DSP22000-ILT

Who Should Attend? – Hardware engineers looking to utilize high-level synthesis

Prerequisites

- C, C++, or System C knowledge
- HDL knowledge
- Hardware design

Software Tools

- Vivado System Edition 2012.2

Hardware

- Architecture: Zynq™-7000 All Programmable SoC and 7 series FPGAs*
- Demo board: None

* This course focuses on the Zynq-7000 All Programmable SoC and 7 series FPGA architectures.

** Check with [Morgan Advanced Programmable Systems, Inc.](http://www.morgan-aps.com) for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the difference between software programming and hardware design
- Model and simulate hardware components using C
- Code hardware components in C for high-level synthesis

Course Outline

- Introduction to Software Programming for Hardware Designers
- C-based Algorithmic Coding for Hardware
- **Lab 1:** High-Level Synthesis of a C Model
- C-based Testbench Coding
- **Lab 2:** Creating a C-based Test Bench

Lab Descriptions

- **Lab 1:** High-Level Synthesis of a C Model – Use various techniques and directives in Vivado HLS to improve design performance. The design under consideration accepts an image in a (custom) RGB format, converts it to the Y'UV color space, and applies a filter to the Y'UV image and converts it back to RGB.
- **Lab 2:** Creating a C-based Test Bench – Develop a verification environment used for testing a C-based design and verification in Vivado HLS. The design under consideration is the same design used in the previous lab, a Y'UV filter.

Register Today

Morgan Advanced Programmable Systems, Inc. (MAPS, Inc.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota and Wisconsin.

Visit morgan-aps.com/training, for full course schedule and training information.



You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent [here](#).

MAPS Inc. Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- MAPS may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is MAPS responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
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