Debugging Techniques Using the ChipScope Pro Tools

FPGA 2

CSP22000-ILT (v1.0)

Course Specification

Course Description

As FPGA designs become increasingly more complex, designers continue look to reduce design and debug time. The powerful, yet easy-to-use ChipScope™ Pro tool solution helps minimize the amount of time required for verification and debug.

This two-day course will not only introduce you to the cores and tools and illustrate how to use the triggers effectively, but also show you effective ways to debug logic and high-speed designs—thereby decreasing your overall design development time. This training will provide hands-on labs that demonstrate how the ChipScope Pro tools can address advanced verification and debugging challenges.

Level – FPGA 2

Course Duration – 2 days

Price – $1,600 or 16 Xilinx Training Credits

Course Part Number – CSP22000-ILT

Who Should Attend? – System and logic designers who want to minimize verification and debug time

Prerequisites

- Basic language concepts for both days
- *Designing with VHDL* or equivalent knowledge of VHDL
- *Designing with Verilog* or equivalent knowledge of Verilog
- Basic FPGA skills for Day 1
- *Essentials of FPGA Design*
- Intermediate FPGA skills for Day 2
- *Designing for Performance* or *Vivado Static Timing Analysis and Xilinx Design Constraints*
- ChipScope Pro Software REL strongly recommended (www.xilinx.com/training/fpga/chipscope-pro-training-video.htm)

Software Tools

- Xilinx ISE® Design Suite: Logic or System Edition 14.2
- ChipScope Pro tool 14.2
- Vivado™ System Edition 2012.2 (optional)

Hardware

- Architecture: N/A*
- Demo boards: Kintex™-7 FPGA KC705 board

* This course does not focus on any particular architecture.

** Check with Morgan Advanced Programmable Systems, Inc. (MAPS Inc.) for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Identify each ChipScope Pro tool core and explain its purpose
- Effectively utilize the ChipScope Pro Analyzer and Vivado analyzer tool
- Implement the ChipScope Pro tool using the CORE Generator™, Core Inserter, and PlanAhead™/Vivado tool flows
- Select effective test points in your design
- Optimize design and core performance when ChipScope Pro tool cores are used
- Execute various techniques for collecting data including
  - File storage
  - Scripting
  - Building custom triggers

Course Outline

Day 1

- How the ChipScope Pro Tool Works
- Inserting the Cores – Inserter Flows: Core Inserter, PlanAhead, Vivado Tools
- **Labs 1 and 2:** Using the Inserter Tool from the PlanAhead Design Environment or Vivado Design Suite
- Instantiating the Cores – CORE Generator Tool Flow
- **Lab 3:** Using the CORE Generator Tool from the PlanAhead Design Environment
- Triggering and Storage
- Visualizing Data – The ChipScope Pro Analyzer Tool
- **Lab 4:** Triggering and Visualization in the Analyzer Tool

Day 2

- Tips and Tricks
- **Lab 5:** Tips and Tricks
- Time for Timing
- Video Demo – Area Groups for Isolation
- Case Studies
- **Lab 6:** FPGA Editor Support for the ChipScope Pro Tool
- Scripting (Optional)*
- Remote Access (Optional)*
- **Lab 7:** Remote Access (Optional)*

* Check with your Authorized Training Provider to confirm whether this content is included with your specific class.

Lab Descriptions

- **Labs 1 and 2:** Using the Inserter Tool from the PlanAhead Design Environment or Vivado Design Suite – Insert ICON and ILA cores into an existing netlist and debug a common problem.
- **Lab 3:** Using the CORE Generator Tool from the PlanAhead Design Environment– Build upon a provided design to create and instantiate a VIO core and observe its behavior using the ChipScope Pro Analyzer tool.
- **Lab 4:** Triggering and Visualization in the Analyzer Tool – Configure triggers and view captured data using the ChipScope Pro Analyzer tool.
- **Lab 5:** Tips and Tricks – Keep time across multiple sample windows and sample across multiple time domains.
- **Lab 6:** FPGA Editor Support for the ChipScope Pro Tool – Change the signals being sampled by an ILA without having to reimplement the design.
- **Lab 7:** Remote Access – Use the ChipScope Pro Analyzer tool to configure an FPGA, set up triggering, and view the sampled data from a remote location.

Register Today

Morgan Advanced Programmable Systems, Inc. (MAPS, Inc.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota and Wisconsin.

Visit **morgan-aps.com/training**, for full course schedule and training information.

Morgan Advanced Programmable Systems

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

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