

### Course Description

In this two-day course, you will learn how to employ serial transceivers in your 7 series or UltraScale™ FPGA or MPSoC design. You will identify and use the features of the serial transceiver blocks, such as 8B/10B and 64B/66B encoding, channel bonding, clock correction, and comma detection.

Additional topics include use of the Transceivers Wizards, synthesis and implementation considerations, board design as it relates to the transceivers, and test and debugging. This course combines lectures with practical hands-on labs.

**Level** – Connectivity 3

**Course Duration** – 2 days

**Price** – \$1,600 or 16 Xilinx Training Credits

**Course Part Number** – CONN-TRX-ILT

**Who Should Attend?** – FPGA designers and logic designers

#### Prerequisites

- Verilog experience (or the *Designing with Verilog* or the *Designing with VHDL* course)
- Familiarity with logic design (state machines and synchronous design)
- Basic knowledge of FPGA architecture and Xilinx implementation tools are helpful
- Familiarity with serial I/O basics and high-speed serial I/O standards is also helpful

#### Software Tools

- Vivado® System Edition 2016.3
- Mentor Graphics Questa Advanced Simulator 10.4

#### Hardware

- Architecture: 7 series and UltraScale FPGAs
- Demo board: Kintex® UltraScale FPGA KCU105 board or Kintex-7 FPGA KC705 board\*

\* This course focuses on the UltraScale and 7 series architectures.

\*\* Check with [Morgan Advanced Programmable Systems, Inc.](http://www.morgan-aps.com) for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe and use the ports and attributes of the serial transceivers in Xilinx FPGAs and MPSoCs
- Effectively use the following features of the gigabit transceivers:
  - 64B/66B and other encoding/decoding, comma detection, clock correction, and channel bonding
  - Pre-emphasis and receive equalization
- Use the Transceivers Wizards to instantiate GT primitives in a design
- Access appropriate reference material for board design issues involving signal integrity and the power supply, reference clocking, and trace design
- Use the IBERT design to verify transceiver links on real hardware

### Course Outline

#### Day 1

- 7 Series and UltraScale Transceivers Overview
- 7 Series and UltraScale Transceivers Clocking and Resets
- Transceiver IP Generation – Transceiver Wizard
- Lab 1:** Transceiver Core Generation
- Transceiver Simulation

- Lab 2:** Transceiver Simulation
- PCS Layer General Functionality
- PCS Layer Encoding
- Lab 3:** 64B/66B Encoding

#### Day 2

- Transceiver Implementation
- Lab 4:** Transceiver Implementation
- PMA Layer Details
- PMA Layer Optimization
- Lab 5:** IBERT Design
- Transceiver Test and Debugging
- Lab 6:** Transceiver Debugging
- Transceiver Board Design Considerations
- Transceiver Application Examples

### Lab Descriptions

- Lab 1:** Transceiver Core Generation – Use the Transceivers Wizard to create instantiation templates.
- Lab 2:** Transceiver Simulation – Simulate the transceiver IP by using the IP example design.
- Lab 3:** 64B/66B Encoding – Generate a 64B/66B transceiver core by using the Transceivers Wizard, simulate the design, and analyze the results.
- Lab 4:** Transceiver Implementation – Implement the transceiver IP by using the IP example design.
- Lab 5:** IBERT Design – Verify transceiver links on real hardware.
- Lab 6:** Transceiver Debugging – Debug transceiver links.

### Register Today

Morgan Advanced Programmable Systems, Inc. (MAPS, Inc.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota and Wisconsin.

Visit [morgan-aps.com/training](http://www.morgan-aps.com/training), for full course schedule and training information.



You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

### Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent [here](#).

### MAPS Inc. Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- MAPS may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is MAPS responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us [here](#).