Signal Integrity and Board Design for Xilinx FPGAs

Connectivity 3

CONN-SI (v1.0) **Course Specification**

Course Description

Learn when and how to apply signal integrity techniques to high-speed interfaces between Xilinx FPGAs and other components.

This course combines design techniques and methodology with relevant background concepts of high-speed bus and clock design, including transmission line termination, loading, and jitter.

You will work with IBIS models and complete simulations using Mentor Graphics HyperLynx. Other topics include managing PCB effects and on-chip termination.

Level – Connectivity 3

Course Duration – 3 days live instructor led training (in person or online)

Price – $2,400 or 24 Xilinx Training Credits

Course Part Number – CONN-SI

Who Should Attend? – Digital designers, board layout designers, or scientists, engineers, and technologists seeking to implement Xilinx solutions. Also end users of Xilinx products who want to understand how to implement high-speed interfaces without incurring the signal integrity problems related to timing, crosstalk, and overshoot or undershoot infractions.

Prerequisites

- FPGA design experience preferred (*Designing FPGAs Using the Vivado Design Suite 1* (FPGA-VDES1) course or equivalent)
- Familiarity with high-speed PCB concepts
- Basic knowledge of digital and analog circuit design
- Vivado™ tool knowledge is helpful

Software Tools

- Vivado System Edition 2019.1
- Mentor Graphics HyperLynx 8.2.1

Hardware

- Architecture: N/A*
- Demo board: None*

* This course does not focus on any particular architecture.

** Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe signal integrity effects
- Predict and overcome signal integrity challenges
- Simulate signal integrity effects
- Verify and derive design rules for the board design
- Apply signal integrity techniques to high-speed interfaces between Xilinx FPGAs and semiconductor circuits
- Plan your board design under FPGA-specific restrictions
- Supply the FPGAs with power
- Handle thermal aspects

Course Outline

Part 1 – Signal Integrity

- Signal Integrity Introduction
- Transmission Lines
- IBIS Models and SI Tools
- **Lab 1:** Invoking HyperLynx
- Reflections
- **Lab 2:** Reflection Analysis
- Crosstalk
- **Lab 3:** Crosstalk Analysis
- Signal Integrity Analysis
- Power Supply Issues
- Signal Integrity Summary

Part 2 – Board Design

- Board Design Introduction
- FPGA Power Supply
- **Lab 4:** Power Analysis
- FPGA Configuration and PCB
- Signal Interfacing: Interfacing in General
- Signal Interfacing: FPGA-Specific Interfacing
- **Lab 5:** I/O Pin Planning
- Die Architecture and Packaging
- PCB Details
- Thermal Aspects
- **Lab 6:** Thermal Design
- Tools for PCB Planning and Design
- Board Design Summary

Lab Descriptions

- **Lab 1:** Invoking HyperLynx – Become familiar with signal integrity tools. Use HyperLynx for schematic entry, modeling, and simulation. Modify a standard IBIS model to define a driver and then use its stackup editor to define a PCB.
- **Lab 2:** Reflection Analysis – Define a circuit and run various simulations for effects of reflection.
- **Lab 3:** Crosstalk Analysis – Using simulation, analyze circuit topology and PCB data for strategies to minimize crosstalk.
- **Lab 4:** Power Analysis – Estimate initial power requirements using an Excel spreadsheet, then use the Vivado Power Analyzer to accurately predict board power needs.
- **Lab 5:** Pin Planning – Use the PlanAhead software to identify pin placement and implement pin assignments.
- **Lab 6:** Thermal Design – Determine maximum junction temperature and calculate acceptable thermal resistance.

Register Today

Morgan Advanced Programmable Systems, Inc. (Morgan A.P.S.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota, and Wisconsin.

Visit morgan-aps.com/training, for full course schedule and training information.

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

Morgan A.P.S. Course Cancellation Policy

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.

Online training with real hardware

During the Covid-19 period, some companies do not allow their staff to participate in live in-person training.

- Consequently, Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your Xilinx based device quickly and efficiently.