

Course Description

This course is structured to provide designers with an overview of the hard block capabilities for the Zynq® UltraScale+™ RFSoc family. Special emphasis is placed on the Data Converter and Soft-Decision FEC blocks.

Power estimation is covered to help designers identify the power demands of the device in various operating modes. Since the Zynq UltraScale+ RFSoc is both a high-speed and an analog and digital device, proper layout and PCB considerations are also covered.

Level – Connectivity 3

Course Duration – 2 days

Price – \$1600 or 16 Xilinx Training Credits

Course Part Number – CONN-RFSOC-ILT

Who Should Attend? – Hardware designers interested in understanding the architecture and capabilities of the Zynq UltraScale+ RFSoc data converter and SD-FEC hard blocks.

Prerequisites

- Suggested: [Zynq UltraScale+ MPSoC for the System Architect](#)
- Basic familiarity with data converter terms and principles
- Basic familiarity with forward error correction terms and principles

Software Tools

- Vivado® Design Suite 2018.1

Hardware

- Host computer for running the above software*

* This course focuses on the Zynq UltraScale+ RFSoc architecture. Check with [Morgan Advanced Programmable Systems, Inc.](#) for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe in general the new Zynq UltraScale+ RFSoc family
- Identify typical applications for the data converters
- Describe the architecture and functionality of the ADC
- Utilize the ADC via configuration, simulation, and implementation
- Describe the architecture and functionality of the DAC
- Utilize the DAC via configuration, simulation, and implementation
- Identify the requirements and options for data converter PCB designs
- Describe the architecture and functionality of the SD-FEC hard IP
- Utilize the SD-FEC via configuration, simulation, and implementation

Course Outline

- Zynq UltraScale+ RFSoc Overview {Lectures}
- RFSoc ADC {Lectures, Demo, Lab}
- RFSoc DAC {Lectures, Demo, Lab}
- RFSoc Data Converter Design {Lectures, Labs}
- PCB Design for RFSoc Devices {Lectures}
- RFSoc SD-FEC {Lectures, Demo, Lab}

Topic Descriptions

- Zynq UltraScale+ RFSoc Overview – Overview of the Zynq UltraScale+ RFSoc architecture, including brief introductions to RF, data converter solutions, SD-FEC solutions, driver support, and tool support.
- RF-ADC – Covers the basics of ADCs. Reviews ADC architecture, functionality, interfaces, configuration, and driver support.
- RF-DAC – Covers the basics of DACs. Reviews DAC architecture, functionality, interfaces, configuration, and driver support.
- Data Converter Design – Describes common features, the design flow, and utilizing the example design by simulation and implementation.
- PCB Design for RFSoc Devices – Describes power requirements, performing power estimation, and utilizing the power design. Analog signal requirements, PCB materials and layer stackup options, and analog trace design are also covered.
- Soft-Decision FEC – Covers the basics of forward error correction. Reviews SD-FEC architecture, functionality, interfaces, configuration, and driver support.

Register Today

Morgan Advanced Programmable Systems, Inc. (MAPS, Inc.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota and Wisconsin.

Visit morgan-aps.com/training, for full course schedule and training information.



You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent [here](#).

MAPS Inc. Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- MAPS may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.



Designing with the Zynq UltraScale+ RFSoc

Connectivity 3

CONN-RFSOC-ILT (v1.0)

Course Specification

- Under no circumstances is MAPS responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us [here](#).