Designing with the Zynq UltraScale+ RFSoC

CONN-RFSOC (v1.0)

Course Specification

Course Description

This course provides an overview of the hard block capabilities for the Zynq® UltraScale+™ RFSoC family with a special emphasis on the RF Data Converter and Soft-Decision FEC blocks.

The focus is on:

- Describing the RFSoC family in general
- Identifying applications for the RF Data Converter and SD-FEC blocks
- Configuring, simulating, and implementing the blocks
- Verifying the RF Data Converter on real hardware
- Reviewing power estimation to help identify the power demands of the RFSoC device in various operating modes
- Identifying proper layout and PCB considerations since the Zynq UltraScale+ RFSoC is both a high-speed and an analog and digital device

What's New for 2022.1

- *General*
  - Update to Gen3 devices
  - DFE devices added
  - Labs updated to 2022.1 software
- *Frequency Planning Modules*
  - New Frequency Planner tool
  - Practice targets the new tool
- *Data Converter Practice*
  - Updated to 2022.1 software
  - RF data converter design example supported in ILT version only (requires 2020.1 software)

Level – Connectivity 3

Course Details

- 3 days live instructor led training (in person or online)
- 43 lectures
- 8 labs
- 5 demos

Price – $2,400 or 24 Xilinx Training Credits

Course Part Number – CONN-RFSOC

Who Should Attend? – Hardware designers interested in understanding the architecture and capabilities of the Zynq UltraScale+ RFSoC data converter and SD-FEC hard blocks.

Prerequisites

- Suggested: Zynq UltraScale+ MPSoC for the System Architect
- Suggested: Xilinx Rapid Development Embedded Design
- Suggested: C-based Design: High-Level Synthesis with the Vivado HLx Tool
- Basic familiarity with data converter terms and principles
- Basic familiarity with forward error correction terms and principles

Software Tools

- Vivado® Design Suite 2022.1
- Vitis unified software platform 2022.1

Hardware

- Host computer for running the above software
- Zynq UltraScale+ RFSoC ZCU111 board*

* This course focuses on the Zynq UltraScale+ RFSoC architecture. Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe in general the new Zynq UltraScale+ RFSoC family
- Identify typical applications for the RF data converters
- Describe the architecture and functionality of the RF-ADC
- Utilize the RF-ADC via configuration, simulation, and implementation
- Describe the architecture and functionality of the RF-DAC
- Utilize the RF-DAC via configuration, simulation, and implementation
- Identify the requirements and options for data converter PCB designs
- Describe the architecture and functionality of the Soft-Decision FEC hard IP
- Utilize the Soft-Decision FEC via configuration and simulation

Course Outline

- **Zynq UltraScale+ RFSoC Overview**
  Overview of the Zynq UltraScale+ RFSoC architecture, including brief introductions to RF, RF data converter solutions, SD-FEC solutions, driver support, and tool support. {Lectures, Demo}
- **RF-ADC Hardware**
  Covers the basics of RF-ADCs. Reviews RF-ADC architecture, functionality, interfaces, configuration, and driver support. {Lectures, Demo, Lab}
- **RF-DAC Hardware**
  Covers the basics of RF-DACs. Reviews RF-DAC architecture, functionality, interfaces, configuration, and driver support. {Lectures, Demo, Lab}
- **RFSoC Hardware**
  Provides an overview of the ZCU111 board and describes board setup. {Lectures}
- **Data Converter Design**
  Describes common features, the design flow, utilizing the example design by simulation and implementation, and verifying RF data converter functionality on real hardware. Includes practice of using a software driver to modify RF data converter parameters. {Lectures, Labs}
- **Data Converter Practice**
  Provides practical RF data converter experience using the ZCU111 board evaluation tool and RF analyzer tool. Demonstrates a PYNQ-based application to validate QPSK streams. Describes RF data converter frequency planning. Utilizes an RF data converter design example. {Lectures, Practices}
- **PCB Design for RFSoC Devices**
  Describes power requirements, performing power estimation, and utilizing the power design. Analog signal requirements, PCB materials and layer stackup options, and analog trace design are also covered. {Lectures, Demo, Lab}
- **Soft-Decision FEC Hardware**
  Covers the basics of forward error correction. Reviews SD-FEC architecture, functionality, interfaces, configuration, and driver support. {Lectures, Demo, Labs}

AMD XILINX

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Register Today

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Visit **morgan-aps.com/training**, for full course schedule and training information.

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

Morgan A.P.S. Course Cancellation Policy

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.

Online training with real hardware

During the Covid-19 period, some companies do not allow their staff to participate in live in- person training.

- Consequently, Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your Xilinx based device quickly and efficiently.