EX XILINX

CONN-PCIE (v1.0)   **Course Specification**

Course Description

Learn how to implement a Xilinx PCI Express® core in custom applications to improve time to market with the PCIe® core design.

The focus is on:

- Constructing a Xilinx PCI Express system within the customer education reference design
- Enumerating various Xilinx PCI Express core products
- Identifying the advanced capabilities of the PCIe specification

This course also focuses on the AXI Streaming interconnect.

What's New for 2020.2

- All labs have been updated to the latest software versions

Level – Connectivity 3

Course Duration – 2 days live instructor led training (in person or online)

Price – $1,600 or 16 Xilinx Training Credits

Course Part Number – CONN-PCIE

Who Should Attend?

- Hardware designers who want to create applications using Xilinx IP cores for PCI Express
- Software engineers who want to understand the deeper workings of the Xilinx PCI Express solution
- System architects who want to leverage key Xilinx advantages related to performance, latency, and bandwidth in PCI Express applications

Prerequisites

- Experience with PCIe specification protocol
- Knowledge of VHDL or Verilog
- Some experience with Xilinx implementation tools
- Some experience with a simulation tool, preferably the Vivado® simulator
- Moderate digital design experience

Software Tools

- Vivado Design Suite 2020.2

Hardware

- Architecture: UltraScale™ and UltraScale+™ FPGAs
- Demo board (provided during training): Kintex® UltraScale FPGA KCU105 board

* This course focuses on the UltraScale and UltraScale+ architectures. Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Construct a basic PCIe system by:
    - Selecting the appropriate core for your application
    - Specifying requirements of an endpoint application
    - Connecting this endpoint with the core
    - Utilizing FPGA resources to support the core
    - Simulating the design
- Identify the advanced capabilities of the PCIe specification protocol and feature set

Course Outline

Day 1

- Course Introduction
- Xilinx PCI Express Solutions
- Connecting Logic to the Core
- PCIe Core Customization
- **Lab 1:** Constructing the PCIe Core
- Packet Formatting Details
- Simulating a PCIe System Design
- **Lab 2:** Simulating the PCIe Core
- Endpoint Application Considerations
- PCI Express in Embedded Systems
- **Lab 3:** Using the PCI Express Core in IP Integrator

Day 2

- Application Focus: DMA
- **Lab 4:** Exploring Xilinx DMA
- Design Implementation and PCIe Configuration
- **Lab 5:** Implementing the PCIe Design
- Root Port Applications
- Debugging and Compliance
- **Lab 6:** Debugging the PCIe Design
- Interrupts and Error Management
- Course Summary

Lab Descriptions

- **Lab 1:** Constructing the PCIe Core – This lab familiarizes you with the necessary flow for generating a Xilinx Integrated PCI Express Endpoint core from the IP catalog. You will select appropriate parameters and create the PCIe core used throughout the labs.
- **Lab 2:** Simulating the PCIe Core – This lab demonstrates the timing and behavior of a typical link negotiation using the Vivado simulator. You will observe and capture transaction layer packets.
- **Lab 3:** Using the PCI Express Core in IP Integrator – This lab familiarizes you with all the necessary steps and recommended settings to use the PCIe solutions in an IP integrator block design.
- **Lab 4**: Exploring the Xilinx DMA – This lab familiarizes you with all the necessary steps to set up and perform DMA transfers.
- **Lab 5:** Implementing the PCIe Design – This lab familiarizes you with all the necessary steps and recommended settings to turn the HDL source to a bitstream by using the Tandem configuration mode.
- **Lab 6:** Debugging the PCIe Design – This lab illustrates how to use the Vivado logic analyzer to monitor the behavior of the core and a small endpoint application for proper operation.

Register Today

Morgan Advanced Programmable Systems, Inc. (Morgan A.P.S.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota, and Wisconsin.

XILINX

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Advanced Programmable Systems

Designing an Integrated PCI Express System
Connectivity 3

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Visit **morgan-aps.com/training**, for full course schedule and training information.

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund.   Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

Morgan A.P.S. Course Cancellation Policy

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.

Online training with real hardware

During the Covid-19 period, some companies do not allow their staff to participate in live in-person training.

- Consequently, Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs.   This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote.   Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your Xilinx based device quickly and efficiently.