PCIe Protocol Overview

Connectivity 2

PCIE18000-13-ILT (v1.0)

Course Specification

Course Description

This course focuses on the fundamentals of the PCI Express® protocol specification. The typical PCIe architecture, including data space, data movement, and the most commonly used Transaction Layer Packets (TLPs) are covered. Interrupts and error handling are also discussed.

Implementation issues are covered in the two-day *Designing a LogiCORE PCI Express System* course.

Level – Connectivity 2

Course Duration – 1 day

Price – $800 or 8 Xilinx Training Credits

Course Part Number – PCIE18000-13-ILT

Who Should Attend? – FPGA designers, logic designers, and anyone who needs an in-depth knowledge of the PCIe protocol

Prerequisites

- None

Software Tools

- None required
- VCD viewer optional

Hardware

- Architecture: N/A*
- Demo board: None*

* This course does not focus on any particular architecture.

** Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Interpret various transactions occurring on the link
- Describe the layered architecture and the tasks and packet types each is responsible for
- Properly estimate maximum performance of a link
- Illustrate how errors can be communicated within the system
- Explain the relationship between Virtual Channels (VCs) and Traffic Class (TC) and the interaction with flow control credits

Course Outline

- Introduction
- Introduction to the PCIe Architecture
- Review of the PCIe Protocol
- Packet Formatting Details
- **Lab 1:** Packet Decoding
- Packet Routing
- Interrupts and Error Management
- Summary

Lab Descriptions

- **Lab 1:** Packet Decoding – This lab explores what *really* happens on the link between a root complex and the endpoint. Various packets, including the Physical Layer, Data Link Layer, and Transaction Layer packets are explored. Insight as to what is actually transpiring on the lanes becomes a powerful tool for understanding the protocol as well as debugging various link issues.

Register Today

Morgan Advanced Programmable Systems, Inc. (MAPS, Inc.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota and Wisconsin.

Visit **morgan-aps.com/training**, for full course schedule and training information.

Morgan
Advanced Programmable Systems

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

MAPS Inc. Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- MAPS may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is MAPS responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.