

Course Description

This course teaches hardware designers who are new to high-speed memory I/O to design a memory interface in Xilinx FPGAs. It introduces designers to the basic concepts of high-speed memory I/O design, implementation, and debug using Xilinx 7 series FPGAs.

Additionally, students will learn about the tools available for high-speed memory interface design, debug, and implementation of high-speed memory interfaces.

The major memory types covered are DDR2 and DDR3. The following memory types are covered on demand: RDRAMII, LPDDR2, and QDRII+. Labs are available for DDR3 on the Kintex®-7 FPGA KC705 board.

Level – Connectivity 3

Course Duration – 2 days

Price – \$1,600 or 16 Xilinx Training Credits

Course Part Number – CONN-MIF-ILT

Who Should Attend? – FPGA designers and logic designers

Prerequisites

- VHDL or Verilog experience or *Designing with VHDL* or *Designing with Verilog* course
- Familiarity with logic design: state machines and synchronous design
- Very helpful to have:
 - Basic knowledge of FPGA architecture
 - Familiarity with Xilinx implementation tools
- Nice to have:
 - Familiarity with I/O basics
 - Familiarity with high-speed I/O standards

Software Tools

- Vivado® Design or System Edition 2015.1
- Mentor Graphics Questa Advanced Simulator 10.3d
- Mentor Graphics HyperLynx SI 9.x

Hardware

- Architecture: 7 series FPGAs*
- Demo board: Kintex-7 FPGA KC705 board*

* This course focuses on the 7 series architecture.

** Check with [Morgan Advanced Programmable Systems, Inc.](http://www.morgan-aps.com) for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Identify the FPGA resources required for memory interfaces
- Describe different types of memories
- Utilize Xilinx tools to generate memory interface designs
- Simulate memory interfaces with the Xilinx Vivado simulator
- Implement memory interfaces
- Identify the board design options for the realization of memory interfaces
- Test and debug your memory interface design
- Run basic memory interface signal integrity simulations

Course Outline

Day 1

- Course Introduction
- 7 Series FPGAs Overview
- Memory Devices Overview
- 7 Series Memory Interface Resources
- Memory Controller Details and Signals
- MIG Design Generation

- **Lab 1:** MIG Core Generation
- MIG Design Simulation
- **Lab 2:** MIG Design Simulation

Day 2

- Memory Design Implementation
- **Lab 3:** MIG Design Implementation
- Memory Interface Test and Debugging
- **Lab 4:** MIG Design Debugging
- MIG in Embedded Designs
- **Lab 5:** MIG in IP Integrator
- Memory Interface Board-Level Design
- DDR3 PCB Simulation (optional)
- **Lab 6:** DDR3 Signal Integrity Simulation (optional)

Lab Descriptions

- **Lab 1:** MIG Core Generation – Create a DDR3 memory controller using the Memory Interface Generator (MIG) in the Vivado IP catalog. Customize the soft core memory controller for the board.
- **Lab 2:** MIG Design Simulation – Simulate the memory controller created in Lab 1 using the Vivado simulator or Mentor Graphics QuestaSim simulator.
- **Lab 3:** MIG Design Implementation – Implement the memory controller created in the previous labs. Modify constraints, synthesize, implement, create the bitstream, program the FPGA, and check the functionality.
- **Lab 4:** MIG Design Debugging – Debug the memory interface design utilizing the Vivado logic analyzer.
- **Lab 5:** MIG in IP Integrator – Use the block design editor to include the MIG IP in a given processor design.
- **Lab 6:** DDR3 Signal Integrity Analysis – Learn basic signal analysis options to check waveforms and design optimization (optional).

Register Today

Morgan Advanced Programmable Systems, Inc. (MAPS, Inc.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota and Wisconsin.

Visit [morgan-aps.com/training](http://www.morgan-aps.com/training), for full course schedule and training information.



You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent [here](#).

MAPS Inc. Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- MAPS may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is MAPS responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us [here](#).