How to Design a Xilinx Connectivity System in 1 Day

Connectivity 2

CONN13000-ILT (v1.0)

Course Specification

Course Description

This workshop introduces you to fundamental connectivity concepts and techniques for implementation in Xilinx FPGAs. The focus is on fundamental aspects of serial transceivers, PCIe® technology, memory interfaces, and Ethernet MACs.

Only essential theory is introduced in order to lay a foundation for the material and topics covered in this workshop, which complements more detailed training found in subsequent Xilinx courses.

Design examples and labs show components from the Connectivity Targeted Reference Design (TRD). In addition, an IBERT lab is available that highlights the usage of the serial transceivers.

Level – Connectivity 2

Course Duration – 1 day

Price – $800 or 8 Xilinx Training Credits

Course Part Number – CONN13000-ILT

Who Should Attend? – FPGA designers and logic designers

Prerequisites

- VHDL or Verilog experience or *Designing with VHDL* or *Designing with Verilog* course
- FPGA design experience or *Essentials of FPGA Design* course
- Basic understanding of digital and analog circuit design
- Basic understanding of high-speed serial I/O applications

Software Tools

- Vivado® Design or System Edition 2013.2

Hardware

- Architecture: 7 series FPGAs (especially the Kintex-7 FPGA)*
- Demo board: Kintex-7 FPGA KC705 board*

* This workshop focuses on the 7 series architecture.

** C Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the basic functionality and usage of connectivity hard IP
- Describe the basic functionality and usage of connectivity soft IP
- Describe the basic building blocks of the Connectivity Targeted Reference Design
- Apply your knowledge to use the Targeted Reference Design
- Apply your knowledge to modify the Targeted Reference Design for re-use in your own design
- Optimize serial links using the Vivado logic analyzer

Course Outline

- Introduction
- Transceiver Overview
- **Lab 1:** Transceiver Design
- PCI Express Technology Overview
- **Lab 2:** PCIe Design
- Memory Interfaces Overview
- **Lab 3:** MIG Design
- Ethernet MAC Overview
- **Lab 4:** TEMAC Design
- AXI and IP Interface Overview
- Connectivity Applications
- **Lab 6:** IBERT Lab

Lab Descriptions

- **Lab 1:** Transceiver Design – Use the 7 Series FPGAs Transceiver Wizard to create a GTX transceiver IP. Optionally, download onto the development board to verify functionality.
- **Lab 2:** PCIe Design – Introduces the Vivado IP catalog interface for generating the PCIe block design for a Kintex-7 FPGA application. Optionally, verify functionality in a real system.
- **Lab 3:** Memory Interface Design – Create a DDR3 memory controller with the 7 series MIG within the Vivado IP catalog that will be used in a pre-written design. Optionally, download onto the development board to verify functionality.
- **Lab 4:** TEMAC Design – Use the Tri Mode Ethernet MAC IP within the Vivado IP catalog to generate an EMAC application. Optionally, verify functionality in a real system.
- **Lab 6:** IBERT Lab – Use the 7 series FPGAs IBERT design to verify a GTX link on the development board.

Register Today

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Visit **morgan-aps.com/training**, for full course schedule and training information.

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

MAPS Inc. Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
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