Designing with the Versal Adaptive SoC: Serial Transceivers

ACAP-TRX (v1.0)

Course Specification

Course Description

This course provides a system-level understanding of AMD Versal™ adaptive SoC serial transceivers. Transceiver architecture, IP generation, simulation, and implementation are covered. Additional information on PCB design issues is also covered.

The focus is on:

- Constructing a system using Versal device serial transceivers by:
  - Selecting the appropriate IP for an application
  - Configuring Transceivers Wizard IPs
  - Using transceiver IP example designs
  - Simulating and implementing transceiver IPs
- Identifying the advanced capabilities of the serial transceivers, including using IBERT and eye scan options
- Accessing the appropriate reference material for board design issues involving signal integrity, the power supply, reference clocking, and trace design

What's New for 2024.2

- All modules have been updated to the new GT flow
- All labs have been updated to the latest software versions
- New lab: GTM implementation and verification

Level – ACAP 3

Course Details

- 1 day live instructor led training (online or in person)
- 9 lectures
- 4 labs

Price – $800 or 8 AMD Training Credits

Course Part Number – ACAP-TRX

Who Should Attend?

- Hardware designers who want to create applications using serial transceivers
- System architects who want to leverage the key advantages of serial transceivers

Prerequisites

- Knowledge of Verilog or VHDL
- Familiarity with logic design (state machines and synchronous design)
- Some experience with Vivado™ implementation
- Some experience with a simulation tool, preferably the Vivado simulator
- Familiarity with serial I/O basics and high-speed serial I/O standards is also helpful

Software Tools

- Vivado Design Suite 2024.1

Hardware

- Architecture: All Versal adaptive SoC devices
- Evaluation board: Versal VCK190 board

After completing this comprehensive training, you will have the necessary skills to:

- Describe and utilize the building blocks of the serial transceivers in the AMD Versal devices
- Describe and utilize the ports and attributes of the transceivers
- Design, simulate, and implement the transceivers
- Utilize transceiver debugging options
- Identify transceiver use cases
- Describe transceiver board design requirements

Course Outline

Day 1

- **Course Introduction**
  Introduces the course and discusses serial transmission. {Lecture}
- **Serial Transceiver Shared Features**
  Describes the structure and shared features, such as clocking and reset schemes, of the Versal device serial transceivers. {Lecture}
- **Serial Transceiver Architecture**
  Discusses the architecture and functionality of the transmit and receive functional blocks. {Lecture}
- **Transceiver IP Generation**
  Demonstrates usage of the Transceivers Wizard. {Lecture, Lab}
- **Transceiver IP Simulation**
  Covers how to perform transceiver design simulation. {Lecture, Lab}
- **Transceiver IP Implementation**
  Illustrates how to perform transceiver implementation and verification on real hardware. {Lecture, Lab targeting the VCK190 board}
- **Transceiver Use Cases**
  Discusses using the transceivers for several protocol applications, including the PCI Express®, Ethernet, Interlaken, JESD204, and Aurora interfaces. {Lecture}
- **Transceiver Board Design**
  Describes board design issues involving signal integrity, the power supply, reference clocking, and trace design. {Lecture}
- **GTM Transceiver**
  Reviews GTM transceiver-specific design generation, simulation, implementation, and verification on real hardware. {Lecture, Labs targeting the VPK120 board}

Register Today

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- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
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- For additional information or to schedule a private class contact us here.

Online or in person training with real hardware

- Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your Xilinx based device quickly and efficiently.