

ACAP-NOC (v1.0)

Course Specification

Course Description

This course introduces the AMD Versal™ network on chip (NoC) to users familiar with other SoC architectures. Besides providing an overview of the major components in the Versal device, the course illustrates how the NoC is used to efficiently move data within the device.

The emphasis of this course is on:

- Enumerating the major components comprising the NoC architecture in the Versal adaptive SoC
- Implementing a basic design using the NoC
- Configuring the NoC for efficient data movement

What's New for 2024.1

- All labs have been updated to the latest software versions

Level – ACAP 2

Course Details

- 1 day live instructor led training (online or in person)
- 8 lectures
- 3 labs

Price – \$800 or 8 AMD Training Credits

Course Part Number – ACAP-NOC

Who Should Attend? – Hardware developers and system architects—whether migrating from existing AMD SoC devices or starting out with the Versal devices

Prerequisites

- Any SoC or Versal adaptive SoC architecture course
- [Designing with the Versal Adaptive SoC: Design Methodology](#)
- Familiarity with the [Vivado™ Design Suite](#)
- Familiarity with the Vitis™ Unified IDE

Software Tools

- Vivado Design Suite 2024.1
- [Vitis Unified IDE 2024.1](#)

Hardware

- Architecture: Versal adaptive SoCs

After completing this comprehensive training, you will have the necessary skills to:

- Identify the major network on chip components in the AMD Versal architecture
- Include the necessary components to access the NoC from the PL
- Configure connection QoS for efficient data movement

Course Outline

- **Architecture Overview for Existing Users**
Introduces to students who already have familiarity with AMD SoC architectures the new and updated features found in the Versal devices. {Lecture}
- **Versal Adaptive SoCs Compared to Zynq UltraScale+ Devices**
The Versal adaptive SoC has a number of similarities to the Zynq™ UltraScale+™ MPSoC devices. Understanding what is the same, what is different, and what is brand new helps put this powerful new part into context. {Lecture}
- **NoC Introduction and Concepts**

Reviews the basic vocabulary and high-level operations of the NoC. {Lecture, Lab}

- **NoC Architecture**
Provides the first deep dive into the sub-blocks of the NoC and how they are used. Describes how the NoC is accessed from the programmable logic. {Lecture}
- **Design Tool Flow**
Designers come to the Versal devices with different goals. This module explores how traditional FPGA designers, embedded developers, and accelerated system designers would leverage the most appropriate tools. {Lecture}
- **NoC DDR Memory Controller**
The integration between the NoC pathways and the DDR memory controllers must be understood to have efficient data movement on and off chip. This discussion of the NoC's DDR memory controller blocks provides the background for properly selecting and configuring DDR memory and the memory controller for effective use. {Lecture, Lab}
- **NoC Performance Tuning**
Synthesizes everything about the NoC and its DDRMCs, illustrating how to fine tune the NoC for the best performance. {Lecture, Lab}
- **System Design Migration**
Describes how different users will leverage tools and processes to migrate their designs to the Versal devices. {Lecture}

Register Today

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- You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent [here](#).

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- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.

- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us [here](#).

Online or in person training with real hardware

- Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person...for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly as planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your Xilinx based device quickly and efficiently.