Designing with the Versal ACAP: Architecture and Methodology

ACAP-ARCH (v1.0)

Course Specification

Course Description

This course helps you to learn about Versal® ACAP architecture and design methodology.

The emphasis of this course is on:

- Reviewing the architecture of the Versal ACAP
- Describing the different engines available in the Versal architecture and what resources they contain
- Utilizing the hardened blocks available in the Versal architecture
- Using the provided design tools and methodology to create complex systems
- Describing the network on chip (NoC) and AI Engine concepts and their architectures
- Performing system-level simulation and debugging

What's New for 2022.2

- Introduced Versal Premium series and comparison for device resources among different Versal series devices
- Added information on SSI technology considerations for I/O planning
- Updated information on processor virtual counters
- Updated information on the DSP58 supertile
- Added information on AXI streaming (M:N) to multiple NoC destinations
- Introduced the Power Design Manager (PDM) tool for the Versal ACAP
- Added information on the power and thermal checklist
- Updated information on the NoC simulation flow
- Added information on AXI traffic generators
- All labs have been updated to the latest software versions

Level – ACAP 1

Course Details

- 3 days ILT* or 24 hours On-Demand
- 28 lectures
- 10 labs

Price – $2,400 or 24 Xilinx Training Credits

Course Part Number – ACAP-ARCH

Who Should Attend? – Software and hardware developers, system architects, and anyone who wants to learn about the architecture of the Versal ACAP device

Prerequisites

- Comfort with the C/C++ programming language
- Vitis™ IDE software development flow
- Hardware development flow with the Vivado® Design Suite
- Basic knowledge of UltraScale™/UltraScale+™ FPGAs and Zynq® UltraScale+ MPSoCs

Software Tools

- Vivado Design Suite 2022.2
- Vitis unified software platform 2022.2
- PetaLinux Tools 2022.2

Hardware

- Architecture: Versal ACAPs
- Demo board: Versal ACAP VCK190 Evaluation Platform

* The content in this course may exceed 3 days.

Check with Morgan Advanced Programmable Systems, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the Versal ACAP architecture at a high level
- Describe the various engines in the Versal ACAP device
- Use the various blocks from the Versal architecture to create complex systems
- Perform system-level simulation and debugging
- Identify and apply different design methodologies

Course Outline

Day 1

- **Introduction**
  Talks about the need for Versal devices and gives an overview of the different Versal families. {Lecture}
- **Architecture Overview**
  Provides a high-level overview of the Versal architecture, illustrating the various engines available in the Versal architecture. {Lecture}
- **Design Tool Flow**
  Maps the various engines in the Versal architecture to the tools required and describes how to target them for final image assembly. {Lecture, Lab}
- **Adaptable Engines (PL)**
  Describes the logic resources available in the Adaptable Engine. {Lecture}
- **Processing System**
  Reviews the Cortex™-A72 processor APU and Cortex-R5 processor RPU that form the Scalar Engine. The platform management controller (PMC), processing system manager (PSM), I/O peripherals, and PS-PL interfaces are also covered. {Lecture}
- **PMC and Boot and Configuration**
  Describes the platform management controller, platform loader and manager (PLM) software and boot and configuration. {Lecture, Lab}
- **SelectIO Resources**
  Describes the I/O bank, SelectIO™ interface, and I/O delay features. {Lecture}
- **Clocking Architecture**
  Discusses the clocking architecture, clock buffers, clock routing, clock management functions, and clock de-skew. {Lecture, Lab}
- **System Interrupts**
  Discusses the different system interrupts and interrupt controllers. {Lecture}

Day 2

- **Timers, Counters, and RTC**
  Provides an overview of timers and counters, including the system counter, triple timer counter (TTC), watchdog timer, and real-time clock (RTC). {Lecture}
- **Software Build Flow**
  Provides an overview of the different build flows, such as the do it yourself, Yocto Project, and PetaLinux tool flows. {Lecture, Lab}
- **Software Stack**
  Reviews the Versal ACAP bare-metal, FreeRTOS, and Linux software stack and their components. {Lecture}

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- **DSP Engine**
  Describes the DSP58 slice and compares the DSP58 slice with the DSP48 slice. DSP58 modes are also covered in detail. {Lecture}
- **AI Engine**
  Discusses the AI Engine array architecture, terminology, and AIE interfaces. {Lecture}
- **NoC Introduction and Concepts**
  Covers the reasons to use the network on chip, its basic elements, and common terminology. {Lecture, Lab}
- **Device Memory**
  Describes the available memory resources, such as block RAM, UltraRAM, LUTRAM, embedded memory, OCM, and DDR. The integrated memory controllers are also covered. {Lecture}
- **Programming Interfaces**
  Reviews the various programming interfaces in the Versal ACAP. {Lecture}
- **Application Partitioning 1**
  Covers what application partitioning is and how the mapping of resources based on the models of computation can be performed. {Lecture}

Day 3

- **PCI Express & CCIX**
  Provides an overview of the CCIX PCIe module and describes the PL and CPM PCIe blocks. {Lecture, Lab}
- **Serial Transceivers**
  Describes the transceivers in the Versal ACAP. {Lecture}
- **Power and Thermal Solutions**
  Discusses the power domains in the Versal ACAP as well as power optimization and analysis techniques. Thermal design challenges are also covered. {Lecture}
- **Debugging**
  Covers the Versal ACAP debug interfaces, such as the test access port (TAP), debug access port (DAP) controller, and high-speed debug port (HSDP). {Lecture, Labs}
- **Security Features**
  Describes the security features of the Versal ACAP. {Lecture}
- **System Simulation**
  Explains how to perform system-level simulation in a Versal ACAP design. {Lecture, Lab}
- **Board System Design Methodology**
  Describes PCB, power, clocking, and I/O considerations when designing a system. {Lecture}
- **System and Solution Planning Methodology**
  Describes design partitioning, power, and thermal guidelines. Also reviews system debug, verification, and validation planning. {Lecture}
- **Hardware, IP, and Platform Development Methodology**
  Describes the different Versal ACAP design flows and covers the platform creation process using the Vivado IP integrator, RTL, HLS, and Vitis environment. {Lecture, Lab}
- **System Integration and Validation Methodology**
  Describes different simulation flows as well as timing and power closure techniques. Also explains how to improve system performance. {Lecture}

Register Today

Morgan Advanced Programmable Systems, Inc. (Morgan A.P.S.) delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota, and Wisconsin.

Visit **morgan-aps.com/training**, for full course schedule and training information.

Morgan Advanced Programmable Systems

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

Morgan A.P.S. Course Cancellation Policy

- We regret from time-to-time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- Morgan A.P.S. may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is Morgan A.P.S. responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.

Online training with real hardware

During the Covid-19 period, some companies do not allow their staff to participate in live in-person training.

- Consequently, Morgan Advanced Programmable Systems, Inc. has set up a training VPN where engineer participants can take classes online using the same computers and devCards used during in-person training.
- Even better, and upon request, you can use these computers after hours on training days to experiment with labs. This is not possible for in-person training.
- Additionally, just like in-person training, the laptops and devCards, tools, OS, and licensing are set up in advance.
- In some ways, live online-training is better than in-person…for example, you can grant the instructor permission to look at your Vivado, PetaLinux terminal, or Vitis for extended periods of time if your lab is not going exactly has planned to a missed step.
- This is often more comfortable than two engineers crowding around a laptop screen.
- Taking remote training also allows you to learn some tips and tricks for working remote. Whether your devCard is in the lab down the hall, or across the world via VPN, you can control your Xilinx based device quickly and efficiently.

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